REPORT DOCUMENTATION PAGE

Form Approved
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1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
31-05-2011	Final Report	15 July 2009 - 31 May 2011

4. TITLE AND SUBTITLE

Power MEMS Development

5a. CONTRACT NUMBER

N00014-09-C-0252

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

Drew Hanser, PhD, Program Manager

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

SRI International
333 Ravenswood Avenue
Menlo Park, Ca 94025

8. PERFORMING ORGANIZATION REPORT NUMBER

P19063

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Office of Naval Research
Code 331
875 North Randolph Street
Arlington, VA 22203

10. SPONSOR/MONITOR'S ACRONYM(S)

ONR

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT

Distribution A - Approved for public release; distribution is unlimited

13. SUPPLEMENTARY NOTES

14. ABSTRACT

Final Report

15. SUBJECT TERMS

microelectromechnical system (MEMS), nanocrystalline diamond thin film, microcrystalline diamond substrate, MEMS electron trap

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Drew Hanser
U	U	U	A	44	19b. TELEPHONE NUMBER *(Include area code)* 727-322-7459

Reset

Final Report • May 2011
Covering the Period 15 July 2009 through 31 May 2011

POWER MEMS DEVELOPMENT

Contract N00014-09-C-0252
Submitted in accordance with Deliverable A004 – Final Report
SRI Project P19063

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CONTENTS

TASK 1.1: MEMS RESETTABLE CIRCUIT BREAKER

Contributors: Sunny Kedia, Weidong Wang, Susana Stillwell and John Bumgarner

Deliverables: 10 prototype packed MEMS-based resettable circuit breakers for testing and analysis in ONR laboratories.

1. Objective

The objective of the research in this task was to demonstrate the feasibility of using microelectromechanical system (MEMS) switches as a circuit breaker for electric power management. The concept is to use electrostatically actuated MEMS cantilever switches with integrated bimorph structures to create vertical switches with the capacity to automatically interrupt current flow when over-current situations arise. Using electrostatic actuation, we will be able to reset the circuit breaker following the current interrupt condition. We developed switch designs and manufacturing process flows for device fabrication, and tested and packaged prototype resettable circuit breakers.

2. Approach

The proposed MEMS switch circuit breaker is based on a thermal bimorph cantilever structure. During operation, a voltage is applied between electrodes on the cantilever and the underlying substrate, resulting in pull-in of the cantilever and closure of the switch. The electrostatic pull-in behavior of the cantilever is shown in Figure 1. When the switch closes, contact is made between the circuit on the substrate and a microheater on the cantilever, which closes the circuit. As the current passes through the circuit, the microheater will heat up and generate thermal stress in the cantilever. When the current exceeds a threshold level, the thermal forces in the bimorph overcome the electrostatic actuation force, thereby disconnecting the circuit. In our device, we use silicon (Si) in a silicon-on-insulator (SOI) wafer as the cantilever material (due to its low stress properties) and platinum (Pt) as the heater material. The bonding area, trace area, and electrostatic electrode consist of chromium/gold (Cr/Au).

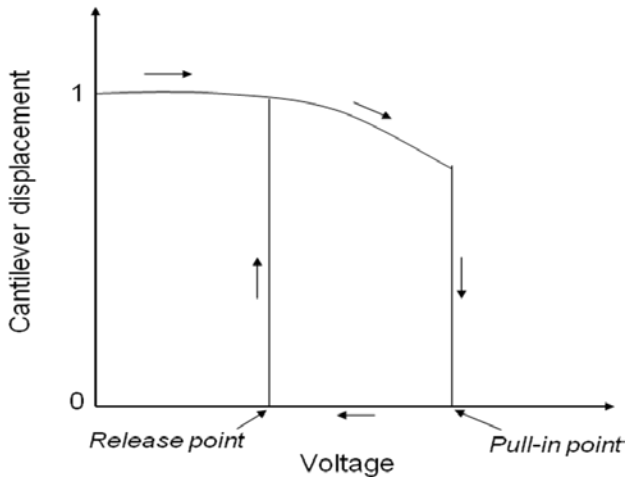


Figure 1: Electrostatic pull-in behavior of the micro-cantilever switch for over-current protection and resetting operation.

3. Simulations

ANSYS Multiphysics 12.0 finite element analysis (FEA) software was used to model and simulate the cantilever electrostatic and structural behavior. We performed coupled-field simulations of the performance of the cantilever to investigate the electrostatic-structural, thermal-electric, and thermal-structural performance of the structure as a function of geometry, materials properties, and operating conditions. Using these simulations, we were able to optimize the design of the cantilever for reduced pull-in voltage, minimization of materials stress, and temperature distribution. Figure 2 shows the simulated maximum temperature and displacement of one of the cantilever designs as a function of input current.

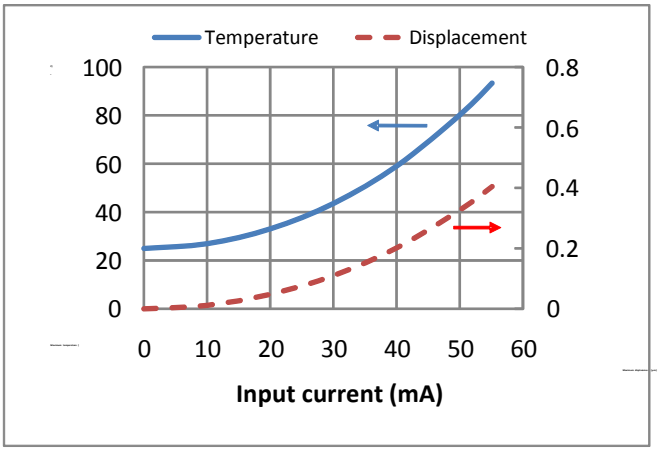


Figure 2: simulated maximum temperature and displacement vs. input current showing a polynomial increasing trend

4. Version 1.0 Design

We incorporated the results from the simulation to design 10 mask layers for the fabrication of the resettable circuit breaker cantilever structure, as summarized in Table 1. In addition, we developed the process flow to fabricate the structures. The device structure involved processing SOI and double-side polished (DSP) Si wafers.

Table 1: Summary of mask layers and purpose for each layer.

Layer	Purpose	Process
Indent	Provides a gap between the SOI contact area and the DSP contact area	Wet etch
Singulation	Etched silicon singulates the chips in 1 x 1 cm or 5 x 5 mm chip size	Dry etch
Metal1	Routing, bond pads, bond metal, bottom electrode, DSP contact area	Wet etch
Metal2	Contact metal on the DSP wafer	Lift off
Release	Etched handle silicon accesses the cantilever and the bond pads	Dry etch
Dielectric	Isolates the heater or the contact area from the top silicon electrode	Dry etch
Metal3	Bond metal, routing connection to the top silicon electrode via metal1	Wet etch
Metal4	Heater layout	Lift off
Metal5	Provides contact metal on the SOI side	Lift off
Structure	Defines the silicon structure in the device layer of SOI	Dry etch

Figure 3 illustrates the mask-level view of the 10 mask layers overlapped. The structures on the top half of the mask were designed for the voltage converter section, and the structures on the bottom half for the resettable circuit breaker section. The mask contains three different 1-cm chip designs and two variations of 5-mm chips. One of the 5-mm chip designs contains the individual resettable circuit breaker configuration with four cantilever designs; in the other 5-mm chip design, the cantilever design was constant and the heater dimensions for both the length and the width were varied. One of the three 1-cm chip designs contains all the different styles of heater and cantilever. The other two 1-cm chip designs contain various styles of breaker with 2x2 and 3x3 arrays to improve the current-carrying capacity.

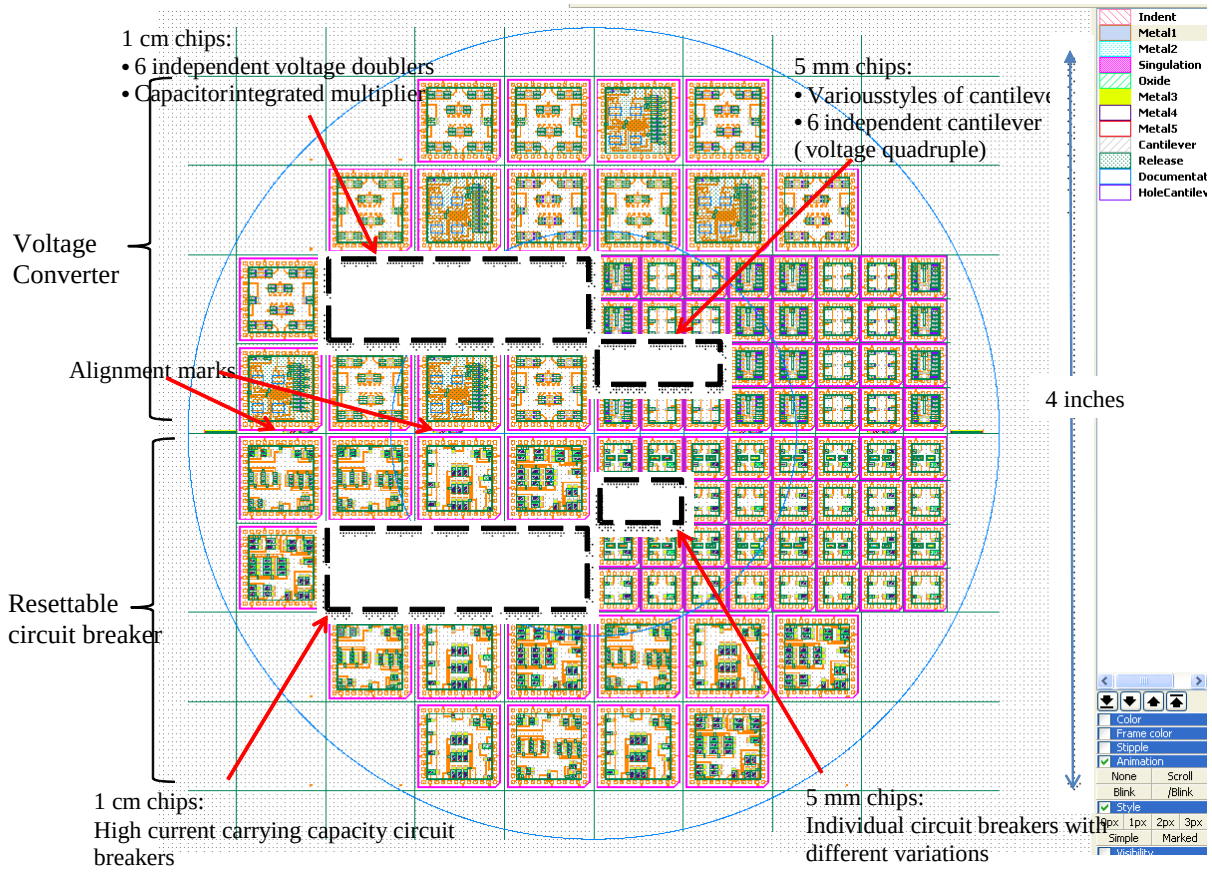


Figure 3: Circuit breaker and voltage converter mask layout.

5. Short-Loop Fabrication Experiments

After the mask design, short loop experiments were completed to solve any fabrication-related issues. We performed the following short-loop experiments:

- **Etch mask for silicon dioxide wet etching:** we verified the use of Cr as a hard mask for silicon dioxide (SiO_2) wet etching. This Cr hard mask was used during the fabrication of the Indent layer in the process flow. The Cr made an excellent hard mask in our process.
- **Au-Au thermocompression bonding:** We developed a process for the gold-gold (Au-Au) thermocompression bonding of the wafers. We verified good wafer bonding and alignment with this experiment. Figure 4 is an image captured with an infrared (IR) camera, showing good bonding alignment following the Au-Au bonding process.

- **Processing of bonded wafer pair:** We investigated the survival of the bonded wafer pair through further processing. Initial cracking issues were identified due to liquid penetration between the wafers during wet processing. We addressed this issue by revising the process flow and eliminating wet processing following wafer bonding. We successfully processed bonded wafers using this modified process, as shown in Figure 5.

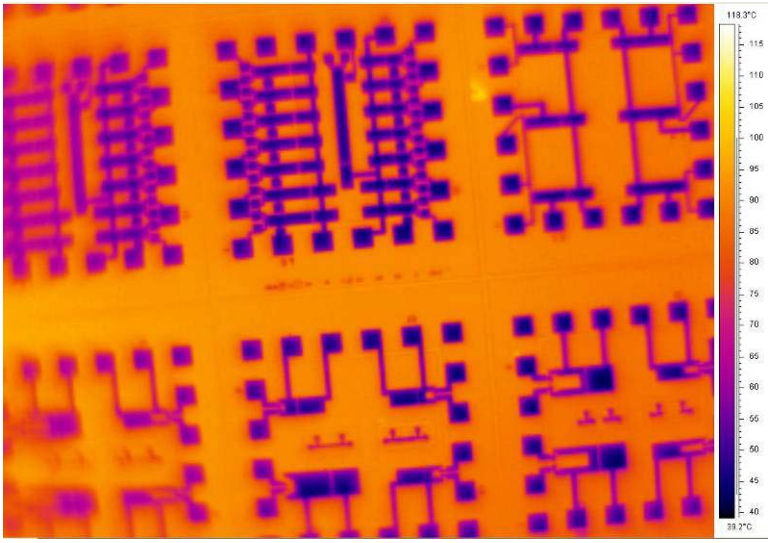


Figure 4: IR image of a bonded wafer pair with good alignment.

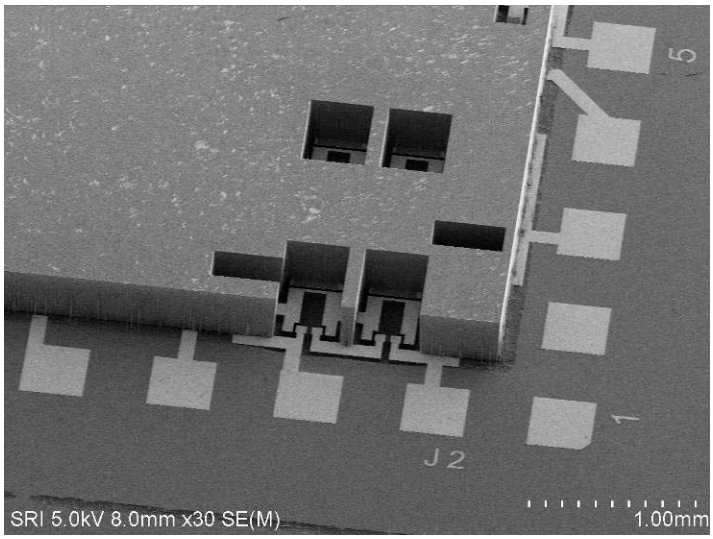


Figure 5: SEM image of a bonded wafer after DRIE.

- **Silicon cantilever processing:** We tested our SOI process flow for fabricating the cantilevers using a silicon-only (no metal or dielectric deposition on the cantilever) short-loop experiment. Following Au-Au wafer bonding, the cantilevers were formed using deep reactive-ion etch (DRIE) processing, and the oxide layer of the SOI wafer was etched using reactive ion etch (RIE) processing. We successfully processed the cantilevers and used this approach for our full wafer fabrication process. During processing, we observed some nonuniformity in the DRIE process across the wafer diameter, which limited the number of usable die for testing. This was an inherent aspect of the process tool and improved only slightly with recipe changes.

6. Version 1.0 Fabrication

With the short-loop experiments completed, we began full-loop wafer processing using the developed process flow (shown in Figure 6), which incorporates two wafers, a silicon DSP wafer, and an SOI wafer, which are bonded together using Au-Au thermocompression bonding

process to complete the devices. At the final step the wafer is singulated into chips using a DRIE process. Here we summarize the results of our initial full-loop wafer processing.

Run 1: We successfully processed the DSP and SOI wafers and bonded them using the Au-Au thermocompression bonding process. Following release of the cantilevers, we measured the position of the cantilevers with scanning electron microscopy (SEM) and a Wyko optical interferometer and found a significant amount of bow away from the substrate due to residual process stress and thermal bimorph stress. We also observed Pt stringers due to a nonoptimized lift-off process. Simulations of the cantilever displacement incorporating process stress of the SiO_2 isolation dielectric on the cantilever resulted in similar displacements to the experimental results, suggesting a cause for the observed deflection.

Run 2: We processed the SOI wafer with silicon nitride (SiN) as the dielectric on the cantilever to reduce the amount of process stress and achieve flatter cantilevers. We also observed reduced Pt stringers by improving the lift-off process. This process run resulted in cantilevers with greatly reduced bow and deflection toward the substrate. We performed electrical measurements on the devices following release.

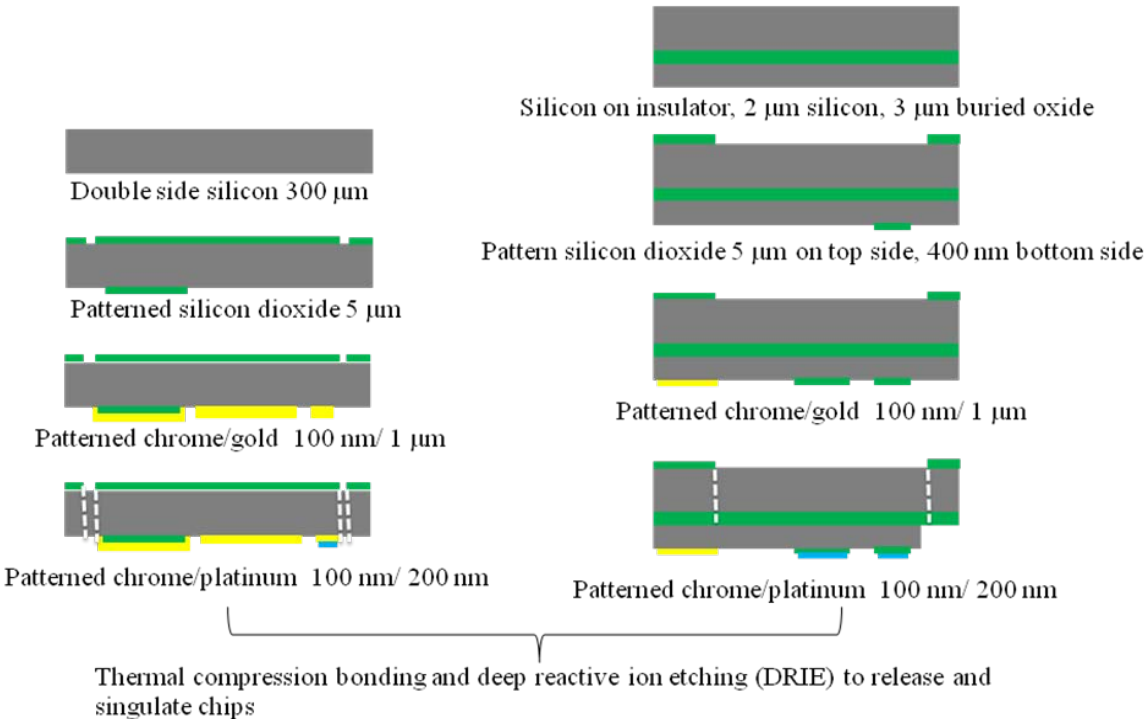


Figure 6: Cross-sectional representation of the process flow.

Run 2 Electrical Measurements: Using a probe station, we applied a voltage to the cantilever electrodes to close the switch and characterize the pull-in behavior (top graph, Figure 7). The pull-in was marked by the change in the circuit resistance following switch closure. The switch released when the electrode voltage was reduced to a point where the circuit opened again. The pull-in voltage ranged from approximately 50 – 60 V for the devices tested. Testing the circuit-breaking capability of the switches involved passing a current through a closed switch and monitoring the circuit resistance while the current was increased. When a critical current

level was obtained, the switch would open and create an open circuit. Testing of the devices on the Run 2 wafer pair resulted in successful operation of several of the resettable circuit breaker devices, proving the proposed concept.

The bottom chart in Figure 7 shows the operation of one of the resettable switches. For H12 Run 1, we closed the H12 switch by applying a voltage (~ 60 V) to the switch actuation electrodes, resulting in a closed circuit at a current of 0 mA through the circuit. Then the voltage was reduced to 50 V. The switch remained closed at this and lower voltage levels, as indicated by the low resistance through the circuit, due to the hysteretic behavior of the electrostatic actuation seen in the top chart of Figure 7. The circuit resistance was monitored while the current was increased. When the current in the circuit reached 55 mA, the Joule heating of the microheater on the cantilever caused the switch to open the circuit, due to the thermal bimorph effect between the Pt heater and the Si cantilever. When the current was returned to 0 mA, the switch remained open, which was verified by the high resistance (> 30 MΩ) of the circuit. This completed the first operation loop of the circuit breaker. The H12 Run 2 was performed using the same procedure as Run 1, and the results were the same as for Run 1, as shown in the bottom chart of Figure 7, except that the pull-in voltage was 78 V for Run 2, compared to 60 V for Run 1, and the holding voltage was 60 V for Run 2, compared to 50 V for Run 1. The performance of the H12 device proved the resettability of the MEMS circuit breaker. Variation in the pull-in voltage between the two runs is thought to be due to a change in the stress in the cantilever structure following heating of the microheater.

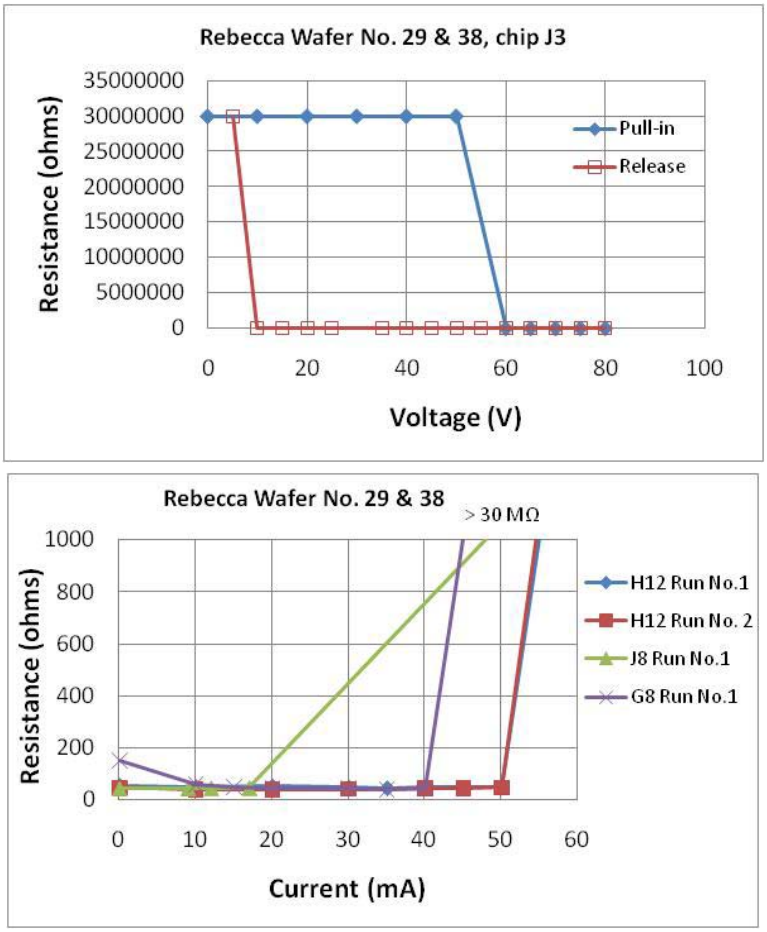


Figure 7: (Top) Pull-in behavior of the circuit breaker cantilevers. The hysteresis observed in the pull-in and release is used for resetting the device. (Bottom) Demonstration of resettable operation of the cantilever following operation (H12 runs 1 and 2).

We examined SEM micrographs of the circuit breaker devices following processing (see Figure 8) and observed that the tips of the released cantilevers touch the substrate. While this does not provide contact to close the switch, it is thought to provide enough deflection of the cantilever to affect the pull-in voltage and performance of the switch. Further evaluation of the cantilevers showed that while the cantilevers were nearly straight, they deflected from the planar position due to an overlap of the Au wafer bond pad at the base of the cantilever (Figure 8b).

This was thought to affect the performance and repeatability of the cantilever. We redesigned the mask to relocate the position of the Au bond pad in the device structure to reduce this effect and produce repeatable switching behavior.

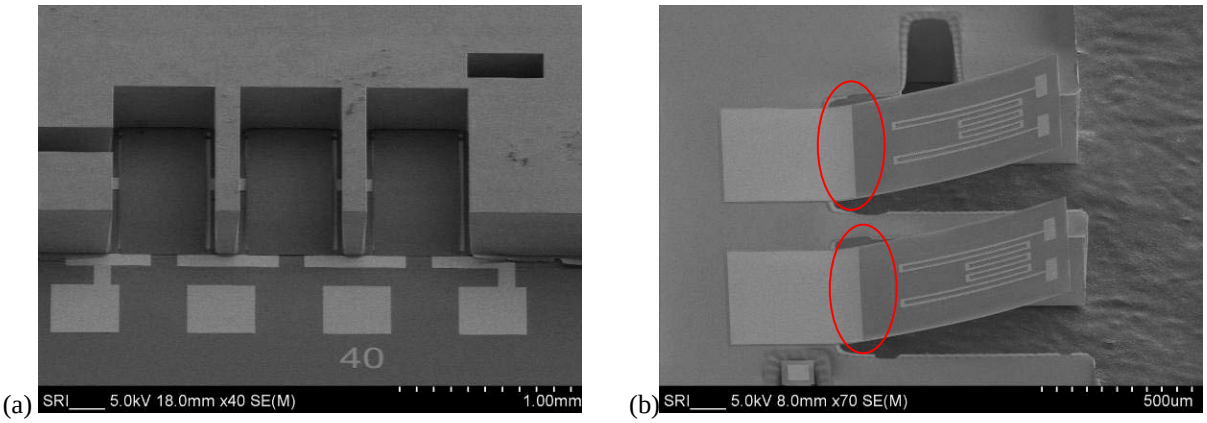


Figure 8: SEM micrographs showing the circuit breaker devices following processing. (a) Released cantilevers in circuit breaker. (b) Detail of a de-bonded device showing bow of the cantilever due to the overlap of the Au bond pad with part of the Si cantilever highlighted by the red ovals.

7. Version 1.1 Design

To address stress issues in the cantilever and improve the functionality of the devices, we modified the Metal3 and Dielectric layers of the Version 1.0 mask set. Figure 9 shows how the Metal3 layer on the released cantilever area was modified to address the stress on the released silicon cantilever. We modified the Metal3 mask such that the metal bond pad does not overlap the released cantilever. We also made modifications to the Dielectric mask by removing the thermal compensation structure following our experimental results, which also reduces the stress in the cantilever.

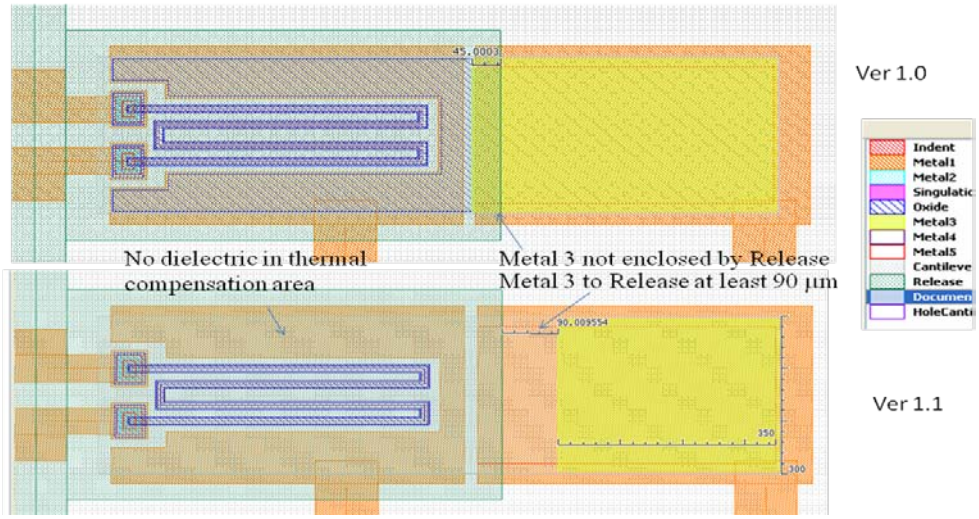


Figure 9: Version 1.1 modification of the cantilever design: the Metal3 (yellow) bond pad is moved away from the release layer (green region) to eliminate the bimorph effect at the base of the cantilever, and the area of the isolation dielectric layer is reduced.

8. Version 1.1 Fabrication

Using the Version1.1 mask set, we processed DSP and SOI wafers using the previous process flow and fabricated circuit breaker devices. Figure 10 is a SEM image of the cantilever that was debonded (similar to Figure 8b). Following the changes in the Metal3 and Dielectric masks, we observed that the released cantilevers were flatter than the previous version. We tested Version 1.1 devices, which exhibited similar results to those of the previous version. However, further analysis of our results and calculations suggested the parasitic capacitance of the devices was extremely high. This effectively reduced the electrostatic voltage being applied on the cantilever, resulting in the high pull-in voltage and variability in our switching results. For future work we will fabricate the devices on high-resistivity Si to reduce the parasitic capacitances.

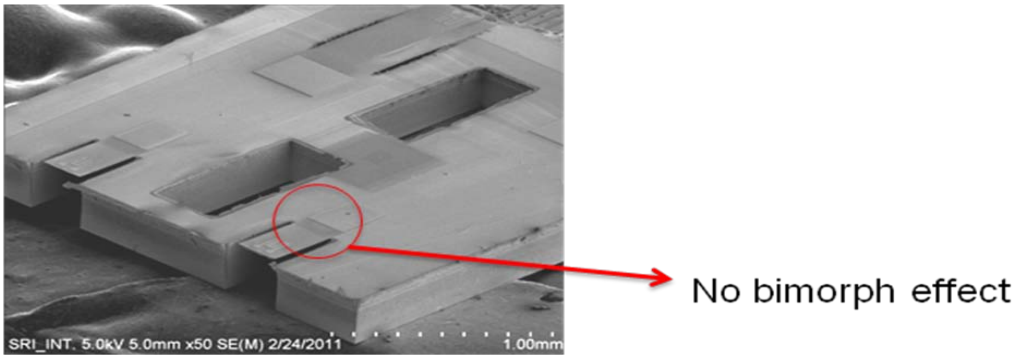


Figure 10: Unbonded resettable circuit cantilever illustrating that there is no bimorph effect as compared to cantilever in Figure 8b.

9. Task 1.1 Conclusions

We developed a MEMS-based resettable circuit breaker for electric power management. Using a thermal bimorph cantilever structure, we created a model to evaluate the electrostatic-structural, thermal-electric, and thermal-structural performance of the structure and created a preliminary device design. We performed several short-loop experiments to optimize the process flow, including wet-etch mask development, Au-Au thermocompression bonding, process optimization of bonded wafer pairs, and cantilever formation processing. We successfully processed devices using our process flow, but bimorph stresses due to choice of materials and cantilever design resulted in bowed cantilevers with significant displacements from the planar cantilever position. Process and design modifications resulted in flatter cantilevers. Experimental results confirmed the proposed and simulated operation principle of the MEMS resettable circuit breaker. The results showed that the switch achieved good contact at an electrostatic actuation voltage of 55 V. The measured circuit breaker current threshold was in the range of 45 – 55 mA. The measured switch-on voltage is twice as high as the calculated pull-in voltage, which was due to curvature of the cantilever in our initial design and a large parasitic capacitance associated with the conductive Si substrate. Thus, it requires higher voltages than suggested by our model to get good switch contact. Further development will focus on reduction of the parasitic capacitance by using high-resistivity Si substrates.

10. References

[1] J. Chen, and C. Liu, “Development and Characterization of Surface Micromachined, Out-of Plane Hot-Wire Anemometer,” Journal of Microelectromechanical Systems, Vol. 12, No. 6, pp. 979-988, 2003.

TASK 1.2: MEMS SWITCH FOR DC-DC VOLTAGE CONVERTERS

Contributors: Sunny Kedia, Weidong Wang, Christel Munoz, Drew Hanser, Shinzo Onishi, Scott Samson and John Bumgarner

Deliverables: Functional MEMS-based DC-DC converter in a vacuum package

1. Objective

The objective of the research in this task was to demonstrate a MEMS switch-based DC-DC voltage converter (VC) by integrating low-voltage electrostatic cantilevers for AC signal generation and DC capacitor charging with vertical microcapacitors for charge storage. The expected input power is 1.5 V and 0.1 mA source(s). The target sample electrical specifications are as follows: output power rate: 12 V 10 μA, maximum output ripple rate: 10 %, electrostatic operation at only 1.5 V source, use of charge transfer or parallel series convertor and integrated topological capacitors.

2. Approach

The device operates in a similar fashion to a Cockroft-Walton (CW) voltage multiplier, but replaces the traditional diodes with MEMS switches to increase efficiency, as shown in Figure 11. We tested the MEMS device's electromechanical behavior, switch contact resistance, reliability, and converter performance using external low-voltage drive signals.

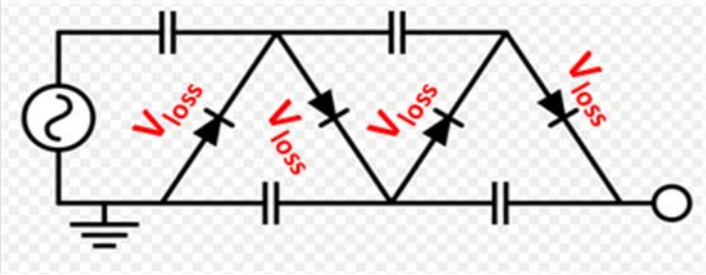


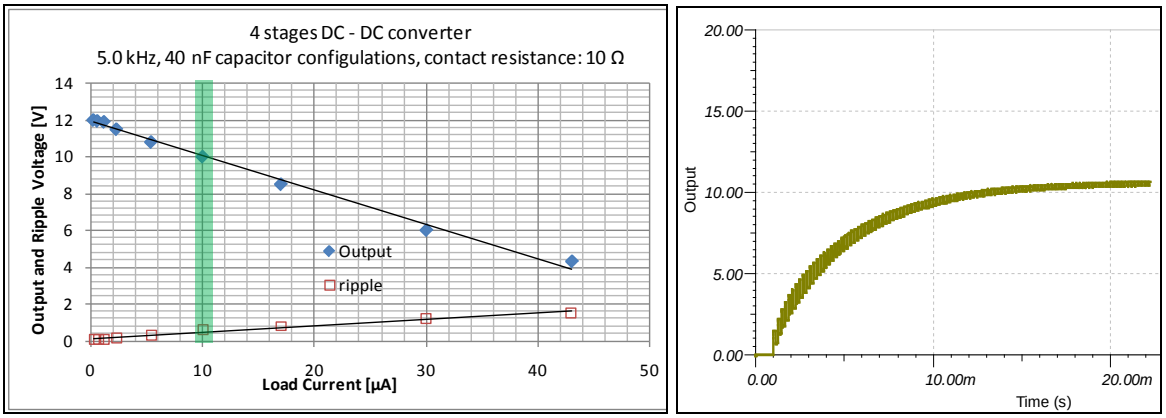
Figure 11: A 2-stage Cockroft-Walton voltage multiplier (4x) [1]. Improved efficiency using a MEMS switch-based approach is achieved by reducing the voltage drop across the diode/switch.

To fabricate the MEMS switches, we developed an integrated process flow. The switches used are conceptually similar to the standard MEMS electrostatic cantilever switch and are fabricated on a microscale on two Si substrates and then assembled using wafer-to-wafer bonding techniques. The contacts are made of platinum family metals, which have excellent fretting corrosion resistance and low stiction. Single-crystal Si and SOI wafers were used to reduce risk of excessive cantilever curvature affecting performance. Device dimensions yielding switch closure near 1.5 V were designed into a mask set. We are including in the design geometric design variations around the target operating point, as well as test structures to account for and to measure variations in actual performance. We investigated MEMS cantilever-, plate- and bench-style switches.

3. Simulations

The performance of a four-stage CW converter, which converts 1.5 VDC to 12V DC, was simulated using a *SPICE* simulation software package. We varied load conditions, switching frequency, and capacitance values, and included a moderately high 10-Ω contact resistance in

some simulations. The effect of contact resistance of 10 Ω for the targeted 10-µA (and higher) load was found to be insignificant. Voltage droop under higher loads was found to be much more significant than ripple (see Figure 12). For less than 10% voltage droop with a 10-µA load and 5-kHz switch operating frequency, the integrated capacitors must be at least 70 nF, and are available in 0201 (0.6 mm x 0.3 mm) surface mount packages. Upon turn-on, the output voltage stabilizes within 20 ms (see Figure 12).



(a) (b)

Figure 12: Four-stage switch-based Cockroft-Walton (CW) voltage multiplier. (a) SPICE simulation results showing output voltage droop and ripple versus load current (green highlight denotes target load). (b) Startup output voltage for circuit with 70-nF capacitor, 5-kHz switch operating frequency, and 10-µA load current.

We also performed a thermomechanical analysis of the cantilever switch design using an ANSYS FEA model. The simulation result shows that the cantilever tip deflects due to residual film stresses and bimorph effects. This analysis was used to inform the cantilever design to minimize deflection.

4. Version 1.0 Cantilever Design

Design

The VC design using cantilever switches was developed in parallel with the circuit breaker devices (see Figure 3). The mask set contains three different 1-cm chip designs and three variations of 5-mm chips. Of the three different 1-cm chip designs, one is a complete 4-stage voltage multiplier (1.5 to 12 V DC/DC converter) with space allocated for bonding commercial 0201 (in dual 0504 packages) capacitors, as part of a multi-chip module, as shown in Figure 13. The other two 1-cm chip designs contain individually addressed voltage multipliers for testing and characterizing the components. One of the 5-mm chip designs contains various styles of cantilever so that we can study electrical and mechanical characteristics such as pull-in voltage, mechanical bow of cantilevers due to stress, and contact resistance versus force. The other two small chips contain individually addressable voltage doublers. A 3-D solid model of the cantilever switch after release is shown in Figure 14.

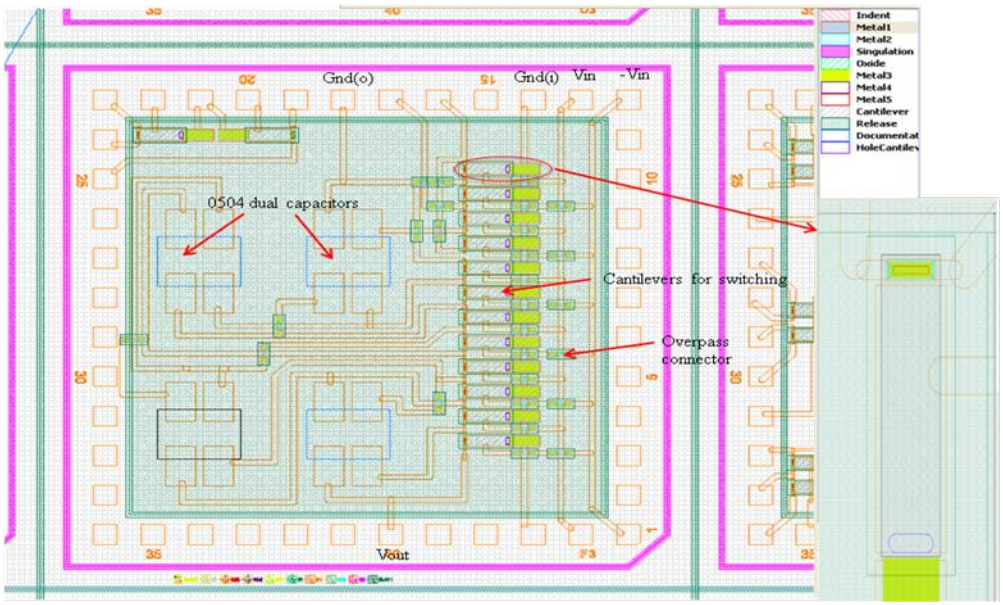


Figure 13: Voltage multiplier multichip module design (1 cm x 1 cm, 1.5 VDC to 12 VDC).

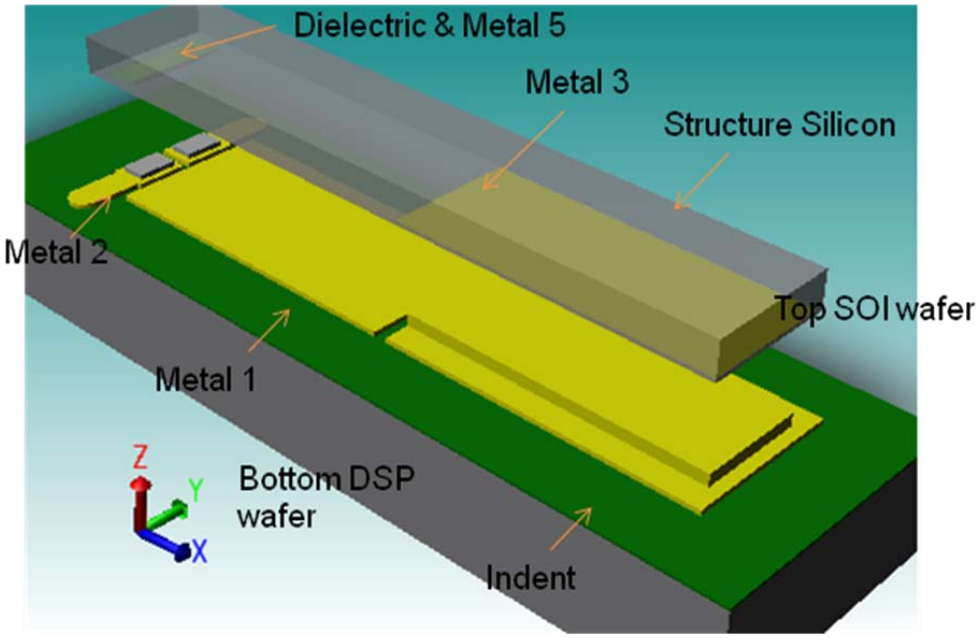
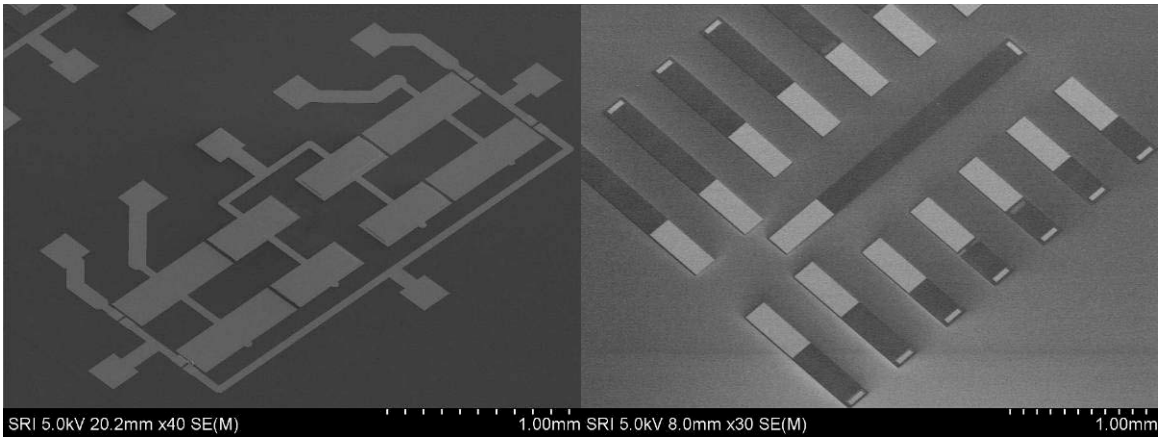


Figure 14: Solid model of the cantilever. The structure silicon is shown as part of the SOI wafer, which is bonded to the bottom DSP wafer.

Fabrication

The short-loop experiments described in Task 1.1 also applied to the development of the VC devices. Following these experiments, DSP and SOI wafers were fabricated using the process flow previously defined. Devices from these wafers are shown in Figure 15. After the individual wafers were fabricated, they were bonded using the Au-Au thermocompression bonding process. Following release of the cantilevers, the switches were tested to measure pull-in voltages and contact resistance.



(a) (b)

Figure 15: a. SEM image of structures fabricated on DSP wafer prior to bonding b. SEM image of structures fabricated on SOI wafer prior to bonding.

Testing

Similarly to the circuit breaker devices, SEM and Wyko optical interferometer measurements showed the VC Version 1.0 cantilevers were bowed following release. This was found to be due to the residual stress in the SiO_2 dielectric on the cantilever (Figure 16). Residual stress measurements in SiN layers showed lower stress values, and we decided to fabricate devices using SiN instead of SiO_2 as the cantilever dielectric. After release of these cantilevers, the cantilevers did not bow at the switch area; however, there was a bow at the tip of the cantilevers.

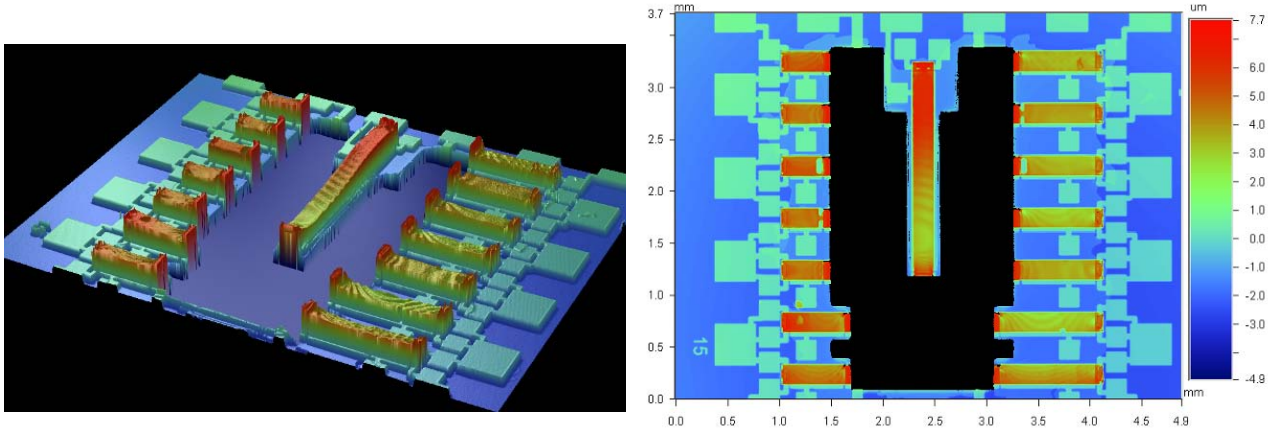


Figure 16: Wyko images of VC cantilevers with SiO_2 dielectric after release.

During testing, several devices showed successful operation when we monitored the resistance of the switch circuit. For these devices, the resistance decreased from ~50 kΩ to 25 Ω at an applied voltage of 15 V. We did not experience consistent results across all the switches. Investigating these issues further, we determined that we had poor ohmic contact to the Si device layer, which was the contact point for the cantilever electrode. As a result, a significant voltage drop occurred at this contact and changed the bias across the switch. We also determined that parasitic capacitance in the Si substrate caused unwanted charging that prevented proper actuation. For further development, we will plan to use silicide contacts for improved ohmic contact behavior and high-resistivity Si substrates to reduce parasitic capacitance.

5. Version 2.0 MEMS Plate Design

In previous development efforts, we have demonstrated MEMS plates with electrostatic actuation at low pull-in voltages (0.4 V -1 .5 V) using a flip-chip bonding method. In this program, we started a parallel effort using this approach to fabricate the voltage converter and address some of the issues with the cantilever design. In this design, we used a Si plate suspended on four sides fabricated from the structure layer of an SOI wafer. The electrical routing and electrostatic drive electrode were pattered on a borosilicate glass wafer, which is thermally matched to the SOI wafer to eliminate misalignment during wafer bonding. We designed a process flow for the Version 2.0 device based on our previous efforts.

The SOI wafer processing is as follows:

- Pattern and DRIE the handle silicon to define the plates, springs, anchors and bond area
- RIE the buried oxide (BOX) to transfer the same pattern
- Deposit, pattern and etch the silicon contact isolation spacer
- Pattern by lift-off and deposit platinum contact metal and gold bonding metal
- Dice the individual chips from the wafer
- Release the plates and springs from the substrate using hydrofluoric-acid-based wet etch.

The glass wafer processing is as follows:

- Pattern and wet-etch the indention for the electrostatic electrode
- Pattern by lift-off and deposit the Pt contact metal, the Au electrical lines, and the Au bond metal
- Dice the glass wafer into individual chips

The two chips are then aligned and bonded together using a flip-chip bonder.

Fabrication and Testing

We completed the fabrication of two SOI wafers and two glass wafers using this design. The SOI wafer contained SiN as the contact dielectric and Pt as the contact metal, with Au as the bond metal. The movable structures and routing electrodes were fabricated using the structure silicon of the SOI wafer. The glass wafer contains Pt as the contact metal and bottom electrode area, and Au features are included for bonding to the SOI chips. We created an indent in the glass wafer using a buffered oxide etchant. This indent defines the gap between the switch and actuator electrodes and is shown in Figure 17. Process development included optimizing the lift-off and release processes, addressing discontinuity in metal coverage on the glass wafer, improving flip-chip alignment, and improving metal adhesion during the release process.

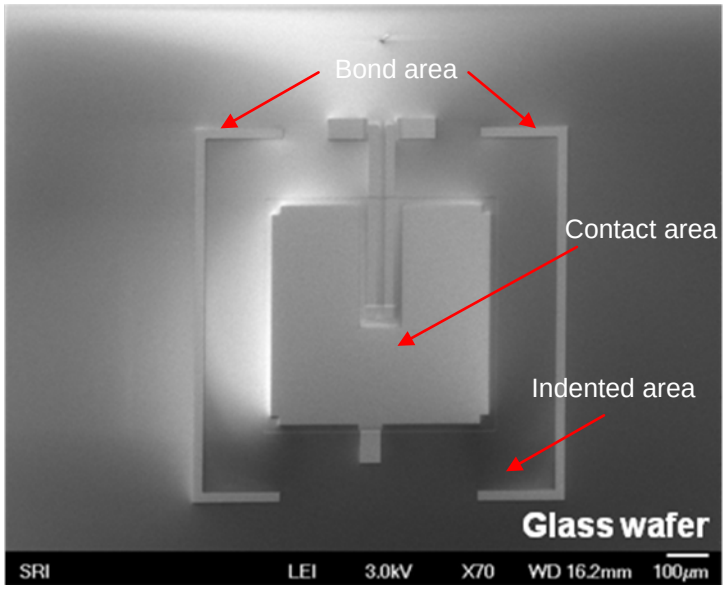
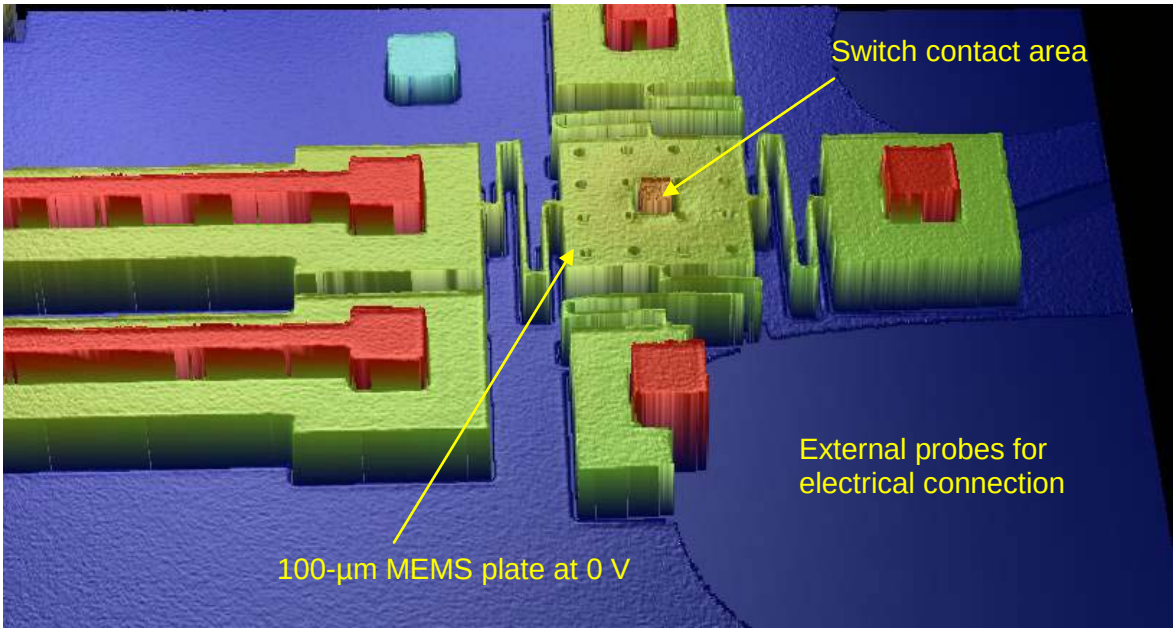


Figure 17: SEM image of a Version 2 glass switch device having a 1-μm indent, Cr/Au as bond metal, and Cr/Pt as contact metal.

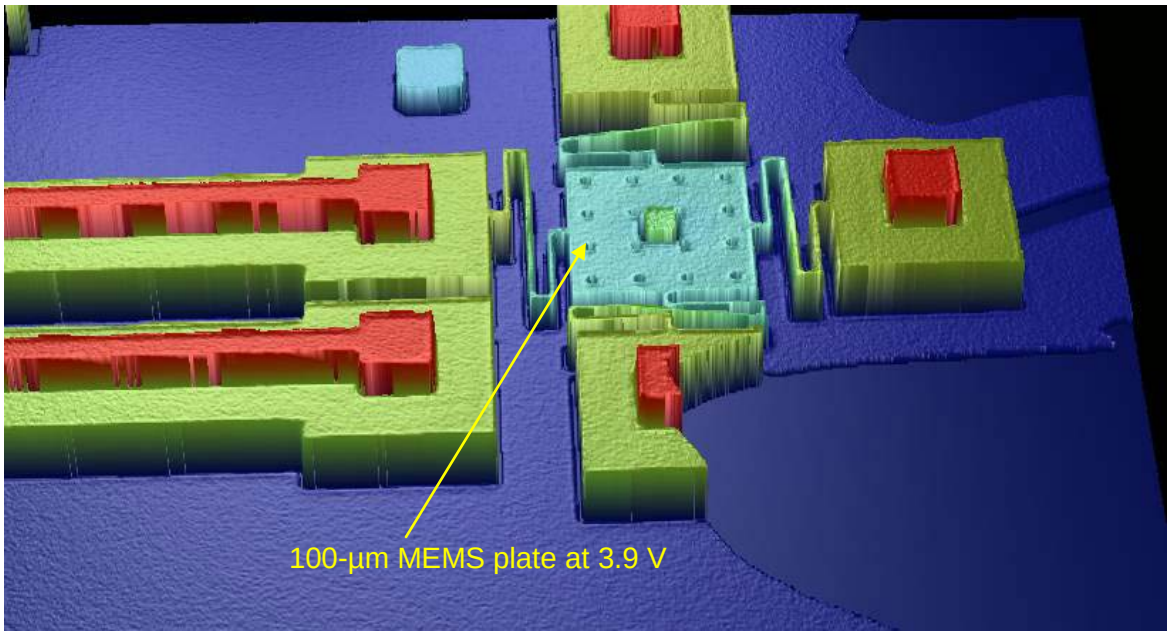
Pull-in Voltage Measurement

We tested the pull-in voltage of the released chips, and the 100-μm-square MEMS plates were measured to pull into the Si substrate at 3.9 V, which is close to the expected pull-in voltage (4.5 V) for this 2-μm-thick silicon having a 1-μm gap between the plate and substrate. An optical profilometer image of one of these devices on a chip is shown in Figure 18. Other chips of different plate styles were tested for pull-in voltages, which were found to be close to the expected values.

During testing, we found that all of the actuating Si structures that were tested moved toward the Si substrate instead of the glass electrode and remained stuck to the Si substrate. Further analysis showed switches that were not tested remained released, indicating that this occurred as a result of the testing. These data suggest that during testing there is an electric potential established between the plate and the Si substrate that allows the plate to move toward the substrate instead of the electrode on the glass substrate. A 1-μm gap between the plate and the substrate allows a small potential to move the plate toward the substrate. Further testing and analysis showed that voltage potentials in this range are developed between the switch and the silicon substrate due to a high contact resistance at the ground contact on the silicon substrate. We designed a new process mask to remove the substrate silicon in the vicinity of the plate using a DRIE process step. This will remove the substrate silicon under the plate, which will allow the MEMS switch plate to move toward the glass electrode. Due to incompatibility of tool operation, we were not able to fabricate and test the wafers.



(a)



(b)

Figure 18: (a) Optical profilometer image of a Version 2 SOI chip at 0 V applied between the top (yellow) and bottom (dark blue) substrate electrodes (b) Optical profilometer image at 3.9 V between the electrodes, which successfully caused the MEMS plate to pull down toward the bottom electrode. For the final working switch, this chip will be bonded to a bonded glass chip having contact and actuation electrodes.

6. Version 3 Switch Design

We developed another approach to address some of the fabrication issues (bonding misalignments, nonuniform DRIE etching, and structure bow due to film stress) experienced in the fabrication of the first versions of the cantilever switches. In addition to the solution paths

mentioned earlier, we developed a completely new process that did not require bonding or DRIE etching. For this new approach, we used surface micromachining to build the switches, layer by layer, on a single substrate. The switch structures comprised a low-stress dielectric anchored at both ends in a bench design to minimize curvature. Since the structural layer was now a dielectric, no DRIE etching of silicon was required. We created elevation by building the switches on top of a sacrificial polyimide layer that was etched away after chip fabrication was completed, resulting in switch structures floating above the substrate. No bonding was required to create a separation gap. Also, because the separation gap height is defined by the thickness of the polyimide layer, it is easily adjustable by changing the thickness of the polyimide. Changing the separation gap height allows for controlled variations of the pull-in voltage.

We fabricated Version 3.0 switches using existing masks, but issues with feature size limitations and routing of electrical connections led us to develop a new mask set designed solely for the new process flow.

Version 3.1 Switch Design

The Version 3.1 design shown in Figure 19 is for a 100-mm substrate and contains approximately 213 chips measuring 5.6 mm x 5.6 mm in size. There are three different switch styles, labeled “H”, “Bench”, and “Meander”. Each chip contains four individual switches, all of the same style. The switches are electrostatically actuated and use DC contact for switch closure. The initial design is based on similar existing switches for RF applications.

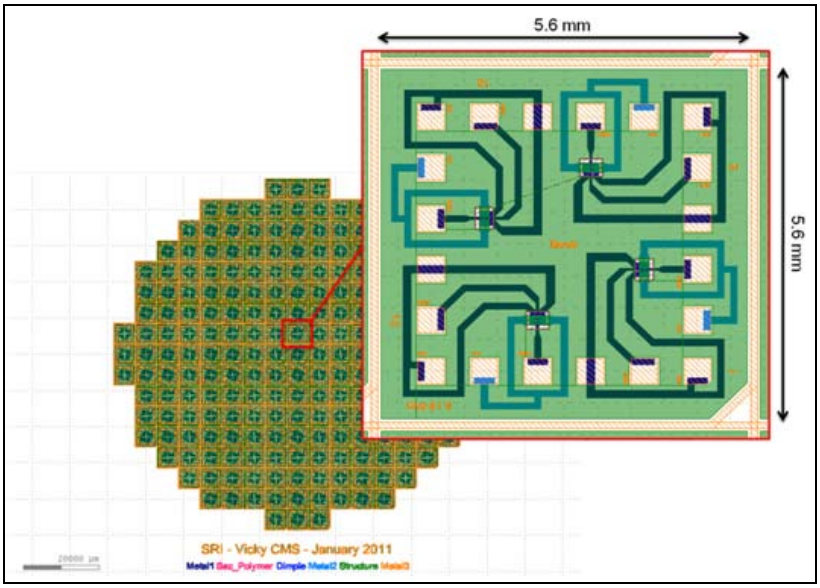


Figure 19: New mask layout designed for a 100-mm wafer, made up of 5.6-mm x 5.6-mm chips.

Figure 20 is a diagram of the electrostatic electrodes, substrate level switch contacts, and floating switch structure for each of the three switch styles. There are electrostatic electrodes on top of the switch structure as well (not pictured). When the switch is actuated and pulls down, a second switch contact on the bottom side of the structure layer bridges the substrate level switch contacts, creating a short circuit which can be measured electrically. As a way of reducing pull-in voltage, we incorporated spring arms in the “H” and “Meander” styles. Additionally, release holes, which allow for the removal of the sacrificial polyimide, also minimize squeeze film damping and reduce switching time.

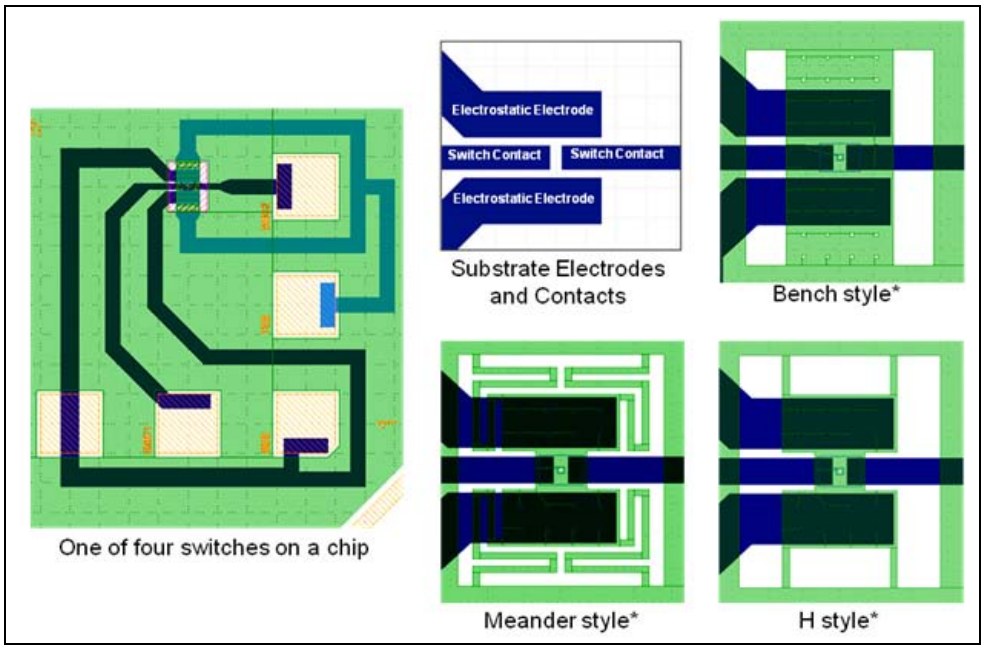


Figure 20: Diagram of the electrostatic electrodes and switch contacts for each switch style.

Version 3.1 Fabrication

The Version 3.1 switch fabrication process uses six masks to pattern four metal layers, two dielectric layers, and one sacrificial polymer layer.

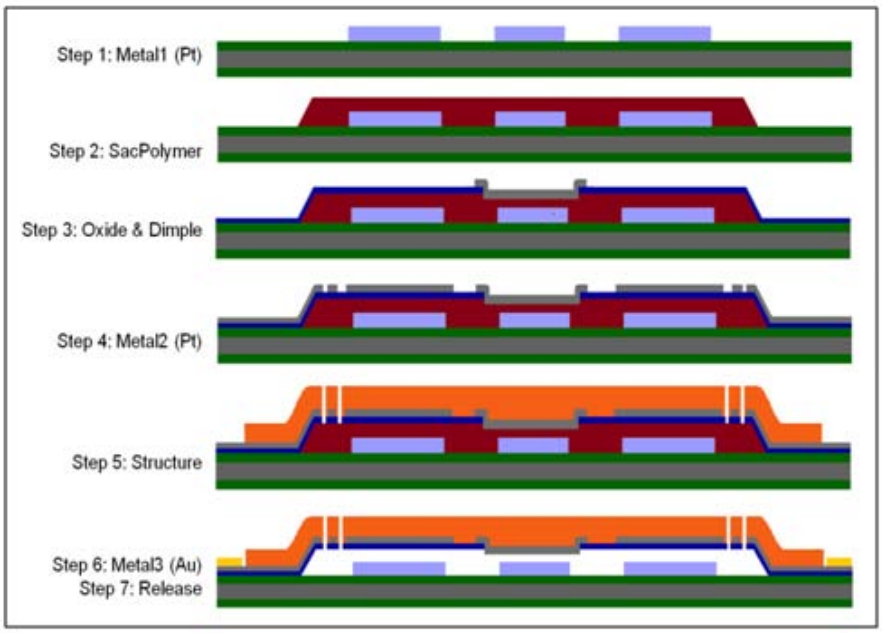


Figure 21 shows a step-by-step cross-section view of the process flow. Process development steps centered on addressing delamination issues with the sacrificial polymer. We achieved the best results by depositing the Metal2 electrode layer on top of the oxynitride Structure layer instead of underneath to eliminate any stresses due to thermal expansion mismatch. We did not observe any delaminations after reordering the process flow.

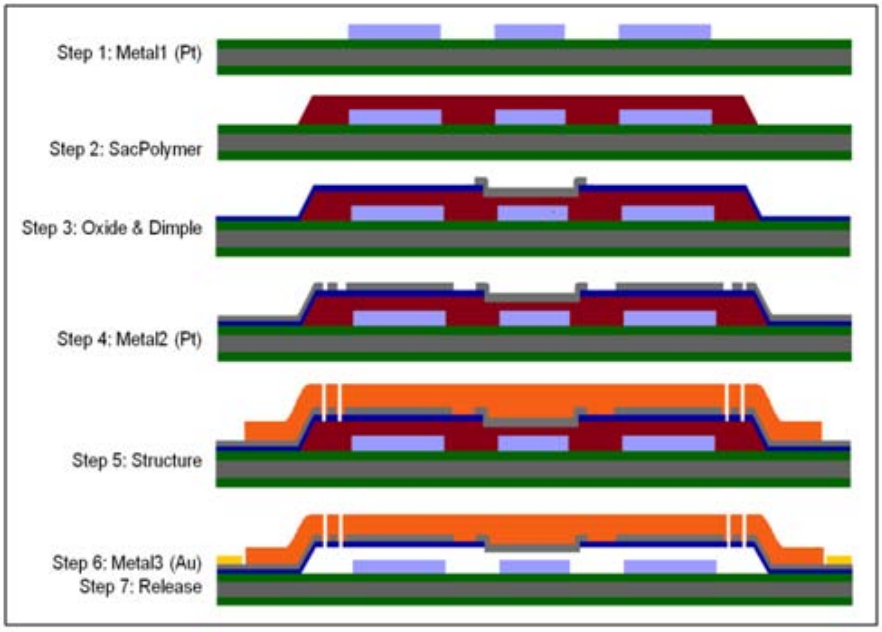


Figure 21: Cross section of the Version 3.1 switch process flow.

After depositing and patterning all the layers, we diced the wafer into individual chips and released the structure layer. The release step was done on individual chips instead of the whole wafer, which allows for better control of the release process and increased yield of successful devices. We used two different release techniques to obtain free-standing switch structures: a combination wet/dry-etch method and a completely dry plasma-etch method. The combination wet/dry-etch release method often left significant amounts of undissolved polymer underneath the switches and also caused more than 50% of the switches to break at their anchor points.

To reduce the likelihood of switches breaking at their anchor points during the wet-etch portion of the combination release, we implemented a completely dry etch using an oxygen plasma. We significantly reduced the number of broken switches with the new release method, and the majority of the switches remained intact after dry plasma release.

Version 3.1 Testing

After we completed fabrication, dicing, and release of the Version 3.1 switches, we measured the degree of curvature of the switches using Wyko optical interferometery, and we tested chips from three wafers for electrostatic pull-in and switch contact closure. For each of the different styles of switches, the bow was ≤ 5 μm across the structures. We tested chips from three wafers for electrostatic pull-in and switch contact closure. For virtually all of the switches, we did not observe the expected change in circuit resistance, indicating issues with switch closure. We performed failure analysis to determine why the majority of the tested Version 3.1 switches did not show a change in resistance and therefore did not indicate successful switch closure. We captured SEM images of deconstructed devices. Based on the SEM results, we attributed failure to insufficient passivation of the Si substrate, poor anchor design, and a non-uniform sacrificial polymer. We completed a mask redesign, Version 3.2, and incorporated filleted anchors, increased anchor size over the edge of the sacrificial polymer, increased electrostatic electrode area to lower pull-in voltage, and bench-style circuit breakers with resistive heaters. Additionally, the mask design required the Metal2 electrode layer to be

deposited after the Structure layer, and we replaced silicon substrates with glass substrates to ensure no parasitic capacitances developed. We fabricated and tested the Version 3.2 switches; optical images are shown in Figure 22.

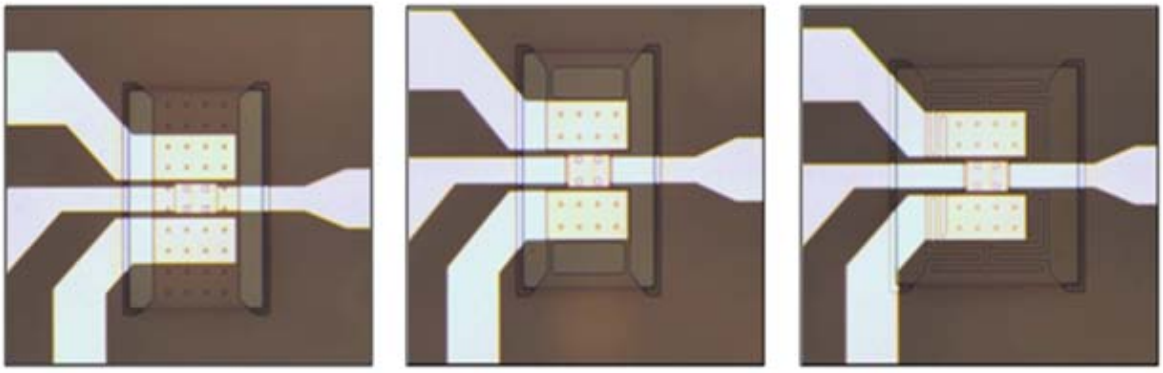


Figure 22: Version 3.2 switches, bench (left), H (middle), and meander (right) style, fabricated on a glass wafer through the Structure layer

Eight chips were tested for electrostatic actuation and a change in resistance to indicate switch closure. A 2X meander-style switch, indicating that the electrostatic electrodes were twice the size of the electrodes in Version 3.1, was permanently stuck down due to stiction. The resistance of the switch was 45.9 Ω , the contact resistance of the metal traces, indicating that the switch was closed. Changes in the switch contact resistance occurred for three of the seven other chips tested. Pull-in voltage was less than 0.5 V for the 2X and 3X electrode styles. However, the resistance values fluctuated from 300 Ω to 12 MΩ due to feedback signals from the Fluke Multimeter used to read out the measured resistances.

The Version 3.2 design resolved most of the issues seen with the previous Version 3.1 switches. The increased size of the anchor resulted in significantly less breakage of the switches. The change from silicon to glass substrates did allow us to observe the release process all the way to completion which took longer than expected. One of the reasons the Version 3.2 switches did not show switch closure may be that the release process was incomplete. Finally, the increased size of the electrostatic electrodes reduced the required pull-in voltage by 2 orders of magnitude, which would now make feasible the use of a standard 1.5-V battery.

7. Task 1.2 Conclusions

Three approaches for fabrication of MEMS switches were taken: (1) a cantilever design and a wafer-wafer bonding approach; (2) a plate design and a chip-level bonding approach, and (3) a bench design with a sacrificial polymer approach. We were able to solve numerous issues that evolved during the fabrication process. After testing we were able to successfully test the switch configuration on Version1.0 devices, where applying 15-V contact resistance varied from open configuration to 25 Ω. Four out of 10 switches illustrated switching characteristics, but we could not process them further in Version1.0 due to tool availability issues. A chip with voltage multiplier devices has been packaged and is used for final demonstration. Version 2.0 had flip-chip alignment issues as well as parasitic issues that are yet to be solved, and Version 3.0 had issues releasing the polymer.

8. References

[1] http://en.wikipedia.org/wiki/File:Cockcroft_Walton_Voltage_multiplier.png

TASK 1.3: DIAMOND HEAT SPREADER OR HEAT SINK FOR HIGH-POWER MEMS SWITCH APPLICATIONS

Contributors: Priscila Spagnol, Drew Hanser, Shinzo Onishi, Sunny Kedia, Weidong Wang, Ben Rossie and John Bumgarner

Deliverables: Prototype device fabricated on a thin film diamond heat spreader layer; individual samples of diamond or other suitable substrates for material evaluation.

1. Objective

The objective of the research in this task was to develop growth processes for diamond thin and thick films and to characterize the properties of the diamond materials. We will investigate the use of these diamond materials in MEMS-based power devices.

2. Approach

We identified the following subtasks in our development approach:

- **Subtask 1: Deposition of diamond film using two approaches.** We developed deposition approaches for thin nanocrystalline diamond (NCD) films and thick free-standing microcrystalline diamond (MCD) films. Our goal was to optimize the deposition recipe in terms of temperature, microwave power, pressure, and gas ratios.
- **Subtask 2: Examine ways to improve nucleation density.** We conducted this subtask using different retreatments such as ultrasonification in different slurries, sample bias, and carbide-forming buffer layers.
- **Subtask 3: Film characterizations.** We characterized the films using a variety of techniques, including AFM, SEM, optical interferometry, and thermal conduction.
- **Subtask 4: Evaluation and selection of the best growth film.** The best films will be used for the consecutive power device fabrication.
- **Subtask 5: Development of integrated process flow.** This subtask included deposition, patterning, and etching to incorporate diamond thin films into the MEMS switch structures.
- **Subtask 6: Feasibility of using diamond film for positron storage.** In this subtask we evaluated the feasibility of incorporating diamond thin films into the positron storage structures walls.

3. Diamond Growth Results

NCD and MCD films were deposited on Si (100) 2–inch-diameter substrates. The wafers were ultrasonicated in a nanodiamond water suspension (1% w/v, 30 nm particle size) for 20 min, followed by ultrasonication in methanol for about 5 min and hot-plate drying at 100 ^{o}C. The NCD film was deposited via microwave plasma chemical vapor deposition (MPCVD) using a Seki Technotron system with a heated stage. The gas chemistry was optimized based on previous work. In this study we evaluated the influence of the microwave power, deposition time, and substrate height effect on the film's uniformity, grain size, and thermal property. Figure 23 shows a Wyko image of one of the NCD samples. Characterization of the NCD films via SEM revealed a grain size ranging from 10 to 30 nm and good grain size uniformity within the sample and from sample to sample. The NCD roughness was on the order of 5 nm for a 1-µm-thick film. We

measured a thickness nonuniformity across the diameter of the substrate of approximately 10%, arising from the uniformity of the plasma in the processing tool. A constant growth rate was observed with increasing growth time. These results suggested that the NCD film can be used to fabricate MEMS devices due to its low roughness, but the nonuniformity of the film across the wafer can be a problem during lithography and etching steps.

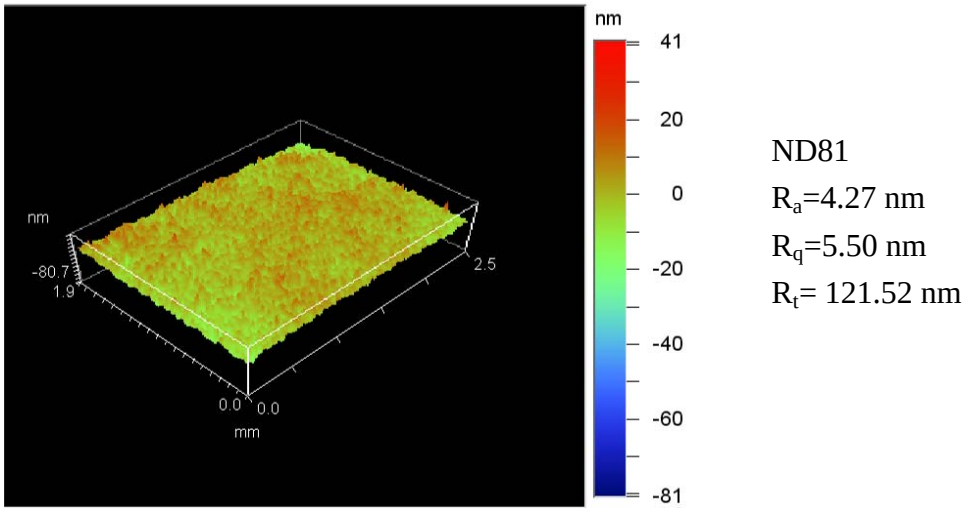


Figure 23: Wyko white light interferometer images of the surface of a NCD film. The Ra surface roughness was measured to be 4.27 nm.

For the deposition of free-standing MCD films we needed to address crack formation in the diamond and the Si substrate, which we observed during our initial growths due to stress generated during the growth and cooling of the film. The thermal stress originates from the difference of coefficient of thermal expansion (CTE) between diamond ($1x10^{-6}$ K^{-1} @ 20 ^oC and $4.7x10^{-6}$ K^{-1} @ 826 ^oC) and Si substrate ($2.49x10^{-6}$ K^{-1} @ 20 ^oC and $4.6x10^{-6}$ K^{-1} @ 826 ^oC). To alleviate the stress, we evaluated a stacked layer composed of a 3-mm Si(100) substrate, 2–6-µm low-pressure chemical vapor deposition (LPCVD) SiO_2, ~2-µm NCD film grown using the heated stage, and finally the thick MCD film grown on the cooled stage. We also found that the control of cracking in the thick MCD films depended on the growth rate of the diamond film, which was controlled by the microwave power. We varied the microwave power from 2.7 to 3.3 kW for the different growth runs; the best growth results for the MCD films were observed at 2.9 kW and 3.0 kW. These conditions gave us a growth rate of ~1.7 µm/hr and crack-free films after cooling and removal of the underlying Si substrate. With this approach, we successfully obtained reproducible, crack-free, thick diamond films. Figure 24 shows representative SEM micrographs of the surface of a MCD film. The surface is significantly rougher than the NCD films due to the larger grain size and greater thickness of the film. As with the NCD films, we noted a thickness nonuniformity of the MCD films across the substrate diameter.

We performed deposition using BEN to investigate improving the nucleation density (ND). As measured by SEM, the ND was estimated to be $<10^6$ cm^{-2} across the substrate, which is significantly lower than the nucleation density observed using the standard ultrasonification process. Process optimization is needed to obtain ND on the order of 10^{12} cm^{-2} or higher, as reported in the literature. Further BEN process development should concentrate on the following parameters: gas flow, substrate temperature, gas chemistry, bias voltage range, and time.

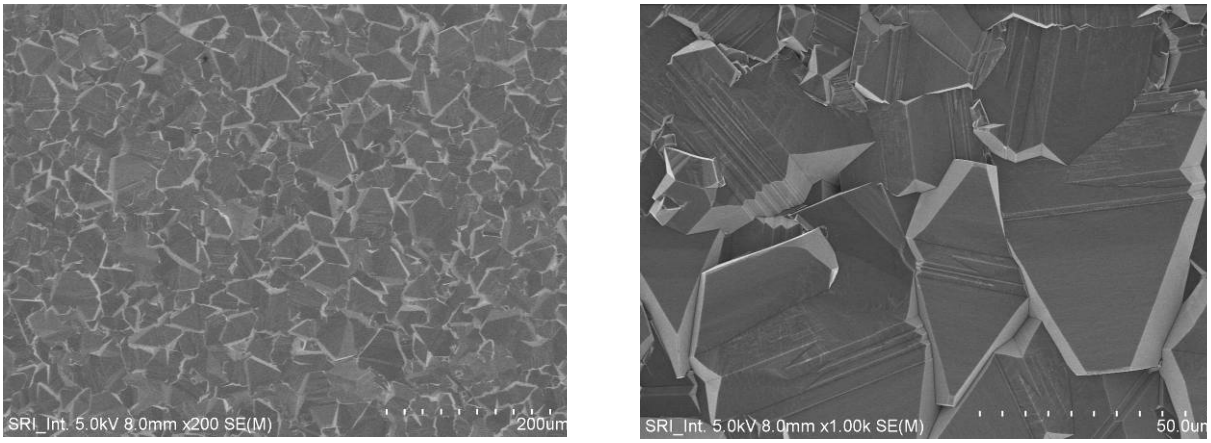


Figure 24: Typical SEM micrographs of an as-grown MCD film (approximately 100 µm thick).

4. Diamond Thermal Conductivity

The main characteristic that needs to be evaluated is the diamond thermal conductivity to allow successful integration of the diamond on the circuit breaker device. CVD diamond is clearly one of the most difficult materials to characterize thermally, not only because of its extreme high conductivity (κ) /diffusivity (D), but also its columnar microstructure and the resulting heterogeneity, which creates a gradient in the local conductivity. The thermal conductivity gradient depends on the direction of heat flow; i.e., the gradient is different for parallel or perpendicular, resulting in a pronounced anisotropy in the local conductivity. Some measurement techniques are more sensitive to this gradient and anisotropy than others. Many different techniques have been used to measure κ and/or D for CVD diamond. For this study we selected the 3-ω method (Figure 25), which uses harmonic Joule heating. A metal resistor, which is deposited on the surface of a dielectric film and serves as a heater, is supplied with a harmonic current to induce Joule heating. The temperature response of the sample is then calculated from the heater's resistance, which is found by measuring the third harmonic of the heater's voltage using lock-in direction. This method, with a simple sample preparation, involves using different heater widths in order to vary the sensitivity to the anisotropy in the film. The benefit of this approach is that the in-plane and out-of-plane thermal conductivity can be measured from one device structure and the same setup, instead of being measured separately.

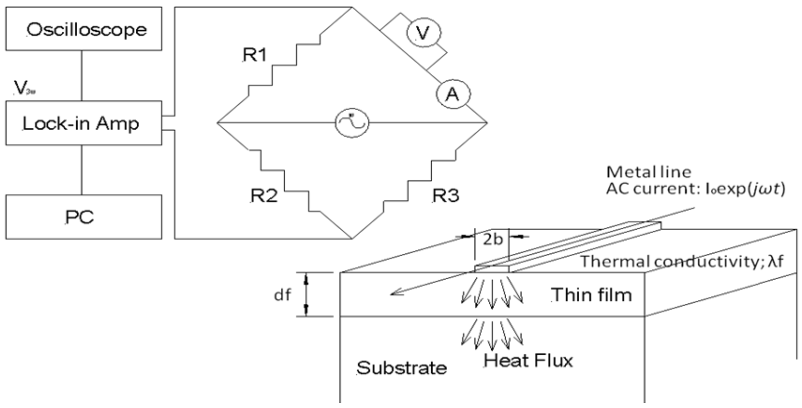


Figure 25: 3-ω method diagram

We developed different resistor patterns (Figure 26) and thicknesses to measure diamond films of various thickness. For thin films on low-conductivity substrates, the resistor thickness needed to be thin (3-6 μm) in order to avoid film/substrate interface effects and to avoid measuring the lower thermal conductivity of the underlying substrate caused by propagation of the thermal wave into the substrate. This would affect our measurement and give a lower effective thermal conductivity in the film.

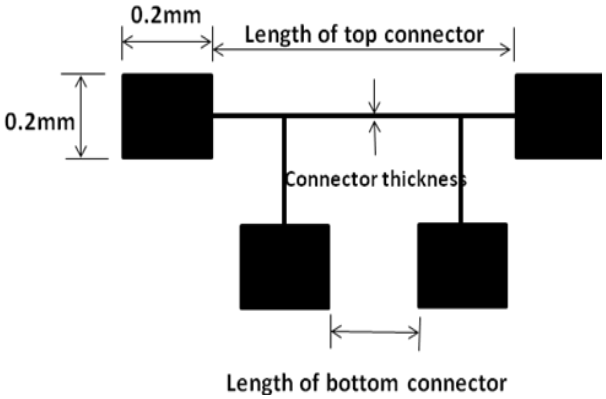


Figure 26: Heat source mask layout for the 3-ω measurements.

For the 3-ω measurements, we developed a process flow for the heater electrode fabrication using Au layers with a thin Cr adhesion layer. We evaluated lift-off and wet-etch processes and found that the lift-off method provided good pattern transfer, relatively smooth line definition, and no undercutting of the pattern. We used the well-known thermal conductivity properties of Pyrex and Si substrates to calibrate the system. We also measured the temperature coefficient (α) of the Au heater sensor in our test structures. A diamond film (~15 μm) polished with RMS ~10 nm on 4-in.-diameter Si substrate was purchased from KINIK for a comparative measurement.

As we developed the 3-ω measurement technique, we encountered several issues that centered on the need to better isolate the resistance measurement of the temperature sensor and improve the measurement of the 3-ω voltage signal (V3ω). To simplify measurements and to acquire better-quality (improved repeatability, lower noise) data, we designed a robust new heater/sensor wire (Version 2). The measurement terminals can be connected using a probe station, a four-point probe, or silver paint, which provides more flexibility. The new wire patterns provided more accurate measurements by eliminating the end effects.

We also developed several iterations of the measurement circuit to improve the measurement of V3ω. A simple circuit was used initially for measuring V3ω across the metal line heater using a lock-in amplifier and a signal generator. An Agilent 33250A signal generator was used to supply the sinusoidal current, and a Signal Recovery 7280 DSP lock-in amplifier was used to measure the nonequilibrium 3-ω voltage of the balanced bridge circuit, which generated the $V_{3\omega}$ voltage signal. The initial circuit configuration did not sufficiently isolate the $V_{3\omega}$ voltage signal from the primary voltage signal (V_{ω}). By upgrading to a 4-terminal bridge circuit, we eliminated the end effect of the metal line heater by allowing the end part of the metal line to be excluded from the measurement. Since the lock-in amplifier has only one pair of differential input terminals, a double differential amplifier front end was required in a 4-terminal bridge circuit operation. A potentiometer was also used to balance the bridge circuit, and signals were fed into two instrumentation differential amplifiers with unity gain. Based on this circuit design, a board was designed to improve the signal from the 3-ω circuits to the bridge circuits using BNC connectors. This 4-terminal bridge circuit configuration enabled us to extract the 3-ω voltage signal from the on-wafer sensor by comparing the signals from two precision operational amplifiers on both sides of the bridge circuit. Additional resistors in the circuit also allow the

circuit to be better balanced. We developed a LabView program for automated measurement of the frequency and voltage data.

A MCD sample previously deposited at 2.9 kW was polished by Applied Diamond, Inc. for our measurements. Following processing, the final thickness of the MCD film ranged from 78 to 131 µm. This sample was patterned for thermal conductivity (TC) measurements using the Au/Cr sensor structure from the Version 2 mask. The MCD film is being characterized for comparison to the diamond sample obtained from a commercial vendor and to evaluate the thermal conductivity for the current baseline growth process. Another sample was also patterned for measurement that consisted of a free-standing MCD film grown on a nanocrystalline diamond (NCD) buffer layer about 2 µm thick. The TC sensors were patterned on the smooth NCD-Si interface following removal of the underlying Si substrate. Thermal conductivity measurements for the different samples are shown in Table 2.

Table 2: Thermal conductivity measurements obtained using the 4-terminal circuit configuration.

Materials	Layer thickness [µm]	Substrate thickness [µm]	Thermal conductivity [W/m·K]
Kinik sample	15	500	869
MCD polished growth side	80	NA	793
MCD silicon side	270	NA	746
Si (100)	500	NA	160
Pyrex	500	NA	1.5
NCD83	8.8	3000	335

5. NCD Stress Measurement

Stress measurements of the NCD film were performed. To fabricate the MEMS test structures, we first patterned anchors on a 3-µm-thick thermal SiO_2 layer, exposing the Si(100) substrate. The wafer was then nucleated by ultrasonication in a nanodiamond 30-nm particle water suspension (1% w/v) for 20 min, followed by ultrasonication in methanol for about 5 min and hot-plate drying at 120 ^{o}C.

Following this step, we deposited NCD films via microwave plasma-enhanced chemical vapor deposition (MPCVD). For these initial experiments we will evaluate the influence of the substrate deposition temperature. The measured residual stress and the calculated thermal and intrinsic stress are shown in Table 3. It should be noted that the measured residual stress can be either compressive or tensile, depending on the hydrogen concentration in the process gas and the deposited temperature. The calculated thermal stress is compressive for all the deposited films.

Table 3: Film stress characterization results.

Substrate temp. C	Residual stress (MPa)	Thermal stress (MPa)	Intrinsic Stress (MPa)
650	-356.6	-554.3	197.7
700	-424.8	-511.4	86.6
750	-233.8	-540.3	306.5

6. Diamond Thermal Simulations

Finite element analysis (FEA) was performed to model and simulate the circuit breaker (Task 1) and evaluate the impact of substituting Si for diamond in the circuit breaker. Using ANSYS FEA software, we performed themoelectrical simulations using the circuit breaker model to examine the thermal effects resulting from substituting the Si base substrate with a microcrystalline diamond substrate (thermal conductivity of 1200 $W \cdot m^{-1} \cdot K^{-1}$ for diamond vs. 150 $W \cdot m^{-1} \cdot K^{-1}$ for Si). This substitution did not result in a significant change in the thermal profile of the cantilever, which had maximum temperatures of 200.6 ^{o}C and 202.1 ^{o}C for the MCD and Si substrates, respectively (Figure 27). This analysis indicated that thermal conductivity in the substrate is not the main regulating factor for reducing the temperature in the cantilever.

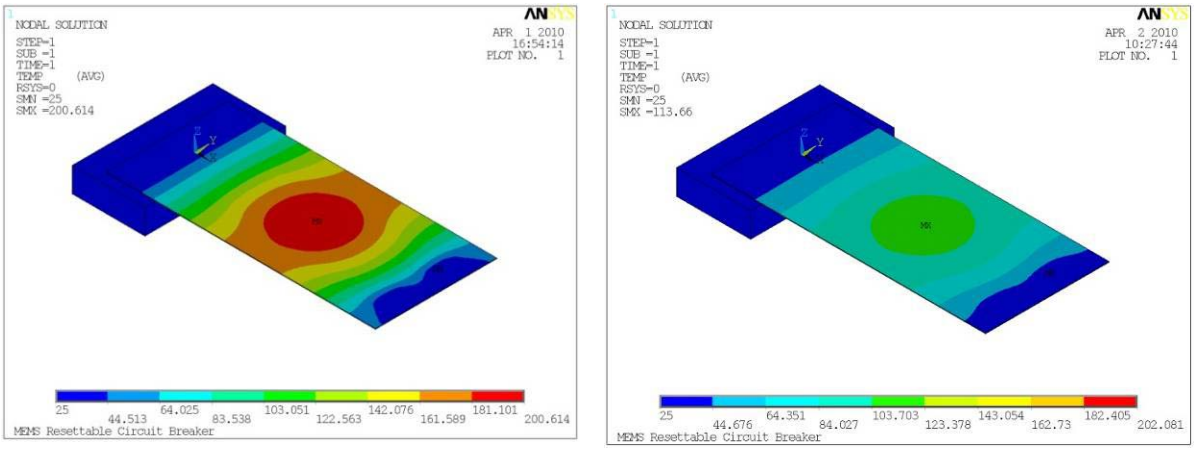


Figure 27: Thermoelectric FEA simulations of the circuit breaker cantilever. (Left): Si cantilever upon a MCD substrate under 25 mA current (214 mW). (Right): MCD cantilever upon a Si substrate under 50 mA current (761 mW). The MCD cantilever removes the heat more effectively.

Propagation of heat through the high thermal impedance between the source of heat in the cantilever and the substrate, which is mounted on a thermal ground plane, has a larger effect on the maximum temperature. This was verified with additional analysis in which we simulated the use of a diamond cantilever in place of the Si cantilever. In this simulation the maximum temperature decreased to 103.7 °C at twice the current. This showed that the diamond cantilever can be used to decrease the temperature of the cantilever, and that the diamond has a much higher power-handling capability than the Si cantilever.

To incorporate the diamond material into the circuit breaker device, we evaluated the process flow for fabrication of the resettable circuit breaker and modified it to accommodate the fabrication of a structural cantilever of NCD instead of SiN or SiO_2, which showed better heat management according to the ANYSIS simulations. We identified a short-loop experiment and initiated one full process run to identify problems before redesigning the mask set. The objective of the short-loop experiment was to check if the rough backside of the single-side polished (SSP) silicon substrate can be used to open the cantilevers using a DRIE etch from the backside. This differs from the current process, which uses DSP wafers. While the short-loop experiment proved that patterning the rough back side of the Si substrate can be managed, it is not a preferred approach. We purchased DSP 2-in. Si(100) substrates to facilitate the fabrication of the devices.

We completed the processing and fabrication of the first resettable circuit breaker wafers with NCD cantilevers (Figure 28). Because we had to change the process steps to accommodate differences in the structure due to the NCD layer, the current mask set does not provide an electrostatically actuated device. But before designing a new mask to allow this characteristic, we processed one wafer to assess the feasibility of the overall fabrication process and to check if other mask design changes would be required. We processed a 2-in.-diameter SSP silicon substrate with the NCD cantilever structures. We then successfully bonded this wafer to a 4-in.-diameter DSP silicon wafer that forms the other half of the device structure, demonstrating the ability to incorporate diamond into the MEMS process flow.

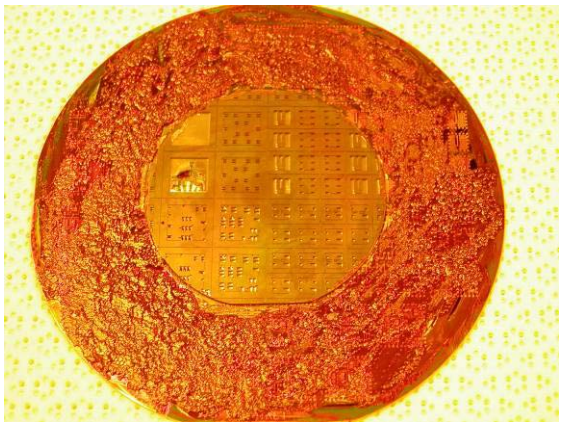


Figure 28: Micrograph of a bonded 2-in. Si-NCD wafer on a 4-in. Si wafer.

7. Diamond Films for Positron Storage

The positron storage development did not reach a maturity where we could incorporate diamond on the fabrication process to evaluate its feasibility, and therefore we were not able to investigate this in the program.

8. Task 1.3 Conclusions

We successfully developed process conditions for NCD and MCD thin and thick films, and we measured the mechanical and thermal properties of these materials. We demonstrated through modeling and simulation that diamond can have a significant benefit in devices by providing a much higher power-handling capability through improved thermal properties, and we developed processes for incorporating diamond into the MEMS process flow.

TASK 2: POSITRON TRAPPING AND STORAGE

Contributors: Ashish Chaudhary, Friso van Amerom, Tim Short

Deliverable: A minimum of four MEMS-based trap structures for RF trapping of electrons

1. Objective

The objective of this research was to develop a method to trap positrons by the use of electrodynamic fields generated by an electrode configuration that would be amenable to miniaturization. This would be an important step toward developing a portable positron source that could be adapted for applications such as antihydrogen production, electron-positron annihilation studies, antimatter initiated fusion/fission, and medical applications (e.g., radiography, positron emission tomography). To demonstrate the validity of the approach, we attempted to trap electrons because they are easier to generate than positrons. In addition, electrons have the same mass but opposite charge of positrons, and thus a proof of concept for trapping electrons should, in theory, be applicable to positrons for the same energy range. Such a trap/storage device could also be used for other charged particles or antimatter with different masses, such as antiprotons, by appropriate adjustments of trapping RF frequency and amplitude. Another feature of RF traps is that they can trap oppositely charged particles simultaneously.

2. Approach

A simplified two-dimensional surface electrode (planar) version of a linear ion trap (LIT) was chosen to show the proof of concept for this method. A brief background about the operation of LITs is included in Section 3 below. We used ion optics simulation software (SIMION) to model different trap geometries to investigate the trapping performance of planar LITs. Simulations of a centimeter-scale planar LIT indicated an optimum trapping frequency in the range of 50-100 MHz and trapping voltage range of 15-30 V_{p-p}. A MEMS approach was adopted to fabricate the planar LIT assembly. Advantages inherent with MEMS technology are the ability to create high-precision electrodes with high repeatability, the possibility for extreme miniaturization, and the potential for batch fabrication. We fabricated a prototype trap in two symmetrical parts and assembled it using a metal spacer in a test setup to achieve the trap geometry shown in Figure 29.

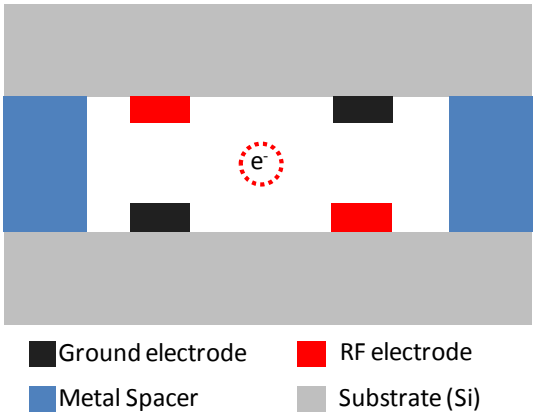


Figure 29: A cross-sectional schematic of a planar LIT showing the arrangement of metal layers used to create a trapping potential at the center of the assembly (thicknesses of surface electrodes are not to scale).

3. Simulations

We modeled LIT geometries with several configurations and scale using the ion optics software SIMION 7.0, a software package originally developed by David Dahl at the Idaho National Laboratory. SIMION is designed primarily to calculate electric fields in complex 2D or 3D configurations of electrodes with static or dynamic electric potentials. Charged particles with

specified initial conditions can be "flown" inside the electrode setup, and trajectories and other particle parameters, such as kinetic energy (KE) and velocity, can be determined and recorded.

We modeled primarily surface-electrode versions of LITs. Figure 30 shows a screen shot of the 3D view of one model. Four electrodes with RF potentials were used to create an oscillating field inside the device. Four shorter electrodes were incorporated on both ends of the RF electrodes, and a small negative potential was applied to restrict the electrons axially. Two mesh-type electrodes were also included in the model for some advanced simulations (discussed in the electron cooling section).

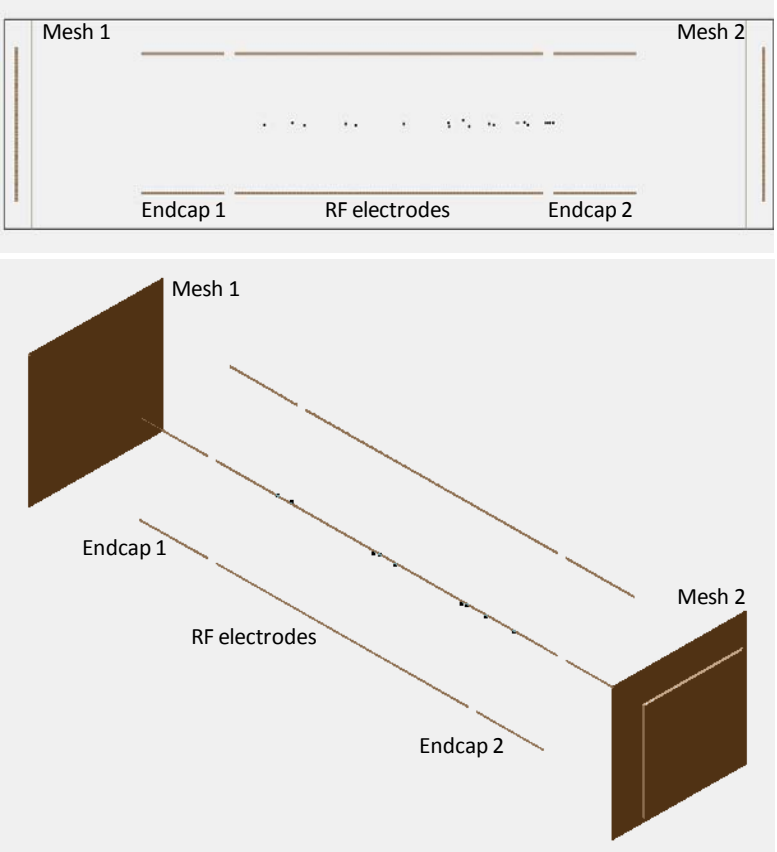


Figure 30: Snapshots of LIT modeled in SIMION.

A user-defined program was written to control the potential applied on the electrodes, randomize the initial conditions of the electrons, and record the trajectory data. Table 4 shows the parameters used for preliminary simulations.

Table 4: Values of operation parameters used in simulations to trap electrons.

Parameter	Value	Units
Electron energy	0.1- 5 (±10%)	eV
RF potential	15-30	V_{p-p}
DC potential	-1	V
Frequency	50-100	MHz
Pressure	10e-7	Torr
Radius	5	mm

In the preliminary simulations, the electrons were created at the center of the trap to determine the trapping performance. Initially, electrons could be trapped for a few milliseconds before their trajectories became unstable and hit the electrodes or the boundary of the potential array. The frequency and amplitude of the potential were then optimized to improve trapping time. It was found that the total trapping time was also limited by the accuracy of trajectory calculations in SIMION, which uses a fourth-order "Runge-Kutta" method to adjust the time steps for particle trajectory calculations. Increasing the precision helped increase the trapping time, but slowed down the simulations to an unrealistic time frame. It was believed that the error in the trajectory calculations during reflections at the end caps was cumulative and was the primary limiting factor for the trapping time (which will not be applicable in real experiments). The best

trapping time recorded for the simulations was 159 ms, but we believe longer trapping times in an experimental setup might be achievable.

Curved Geometries

It was important to investigate the trapping performance using curved geometries to design a more advanced trap to extend the trapping volume. Various curved geometries were simulated and trapping time was recorded (see Figure 31 for examples).

It was observed that electrons could be trapped around curved electrodes (Figure 31 A, B and C). Another interesting design (Figure 31D) was simulated that consisted of two sets of RF electrode separated by a small gap. Electrons were trapped in both electrode sections 1 & 2, and could transit through the gap to be trapped in the next electrode. Such a gap could be used to separate RF electrodes of a relatively longer trap to create multiple trapping sections. Charged particles could then be injected and shifted from individual sections for advanced trapping control.

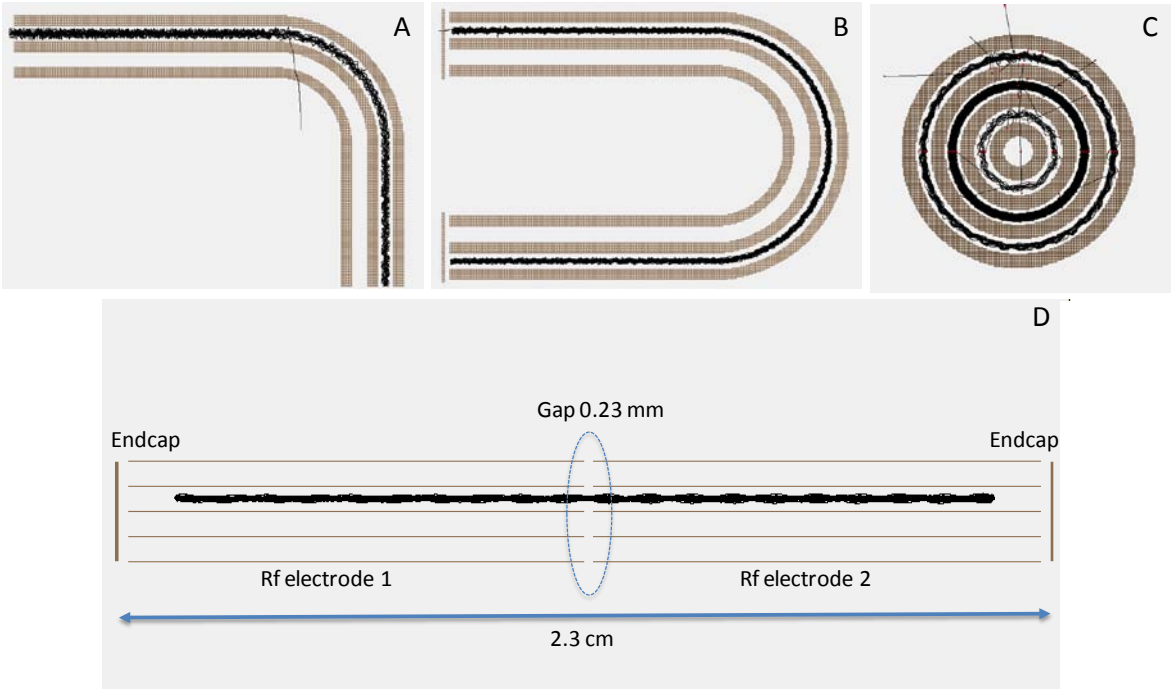


Figure 31: A screen shot of the electrode configuration modeled in SIMION; A: 90° turn; B: 180° turn; C: 360° turn; D: Two straight RF electrodes with a small gap in the center to determine if the electron could transit small gaps and be trapped in the next section of RF electrodes.

Electron Cooling

We carried out initial simulations performed to estimate the optimum trapping voltages and frequency by creating electrons at the center of the trap. To simulate transferring charged particles from an external source (which is more practical for storing positrons and electrons in an actual experimental set up), the model was modified and electrons were initiated from the outside (from the left inFigure 32) of the trap. Based on the electron energy range, the DC potential on the first end cap was adjusted to be approximately at the same level as the electron

energy. This allowed only electrons of slightly higher energy to pass through the potential barrier and enter the trapping region. The potential at the second end cap was adjusted to be slightly higher than the electron energy range. To trap a significant percentage of electrons efficiently using this approach, it is necessary that electrons lose some energy during their first pass through the trapping region, as depicted in Figure 32.

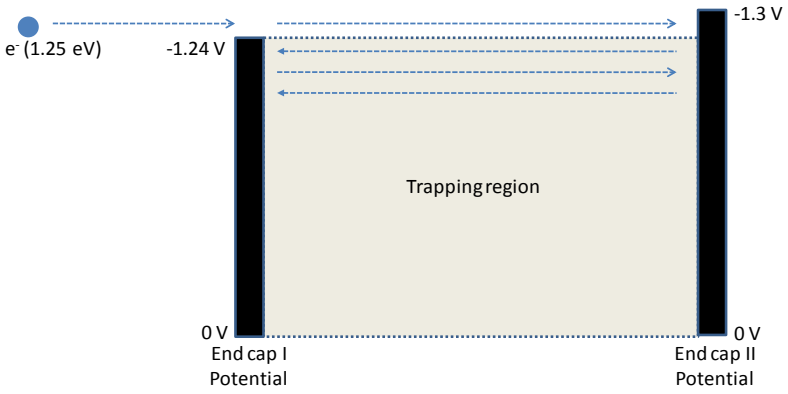


Figure 32: Representation of potential barrier required to trap the electrons axially between the two end-cap electrodes.

One of the most critical challenges in trapping electrons is to reduce their energy (commonly known as "cooling") once they enter the trapping region. Researchers have shown that buffer gases such as nitrogen can be used to cool electrons and positrons. The primary mode of energy loss is inelastic scattering during interaction with nitrogen molecules. However, introduction of buffer gas into the chamber also reduces the mean free path of the electrons and reduces trapping times unless the gas is pumped away very quickly. To attain fast pumping speeds, a large turbomolecular pump would be required, and possibly a complicated differential pump scheme, which are not compatible with constructing a portable instrument.

To investigate an alternative method to reduce the kinetic energy of electrons, we conducted simulations to determine if a short positive voltage pulse on end cap I will slow down electrons once they have entered the trapping region. A user program was written to precisely control the timing of the voltage pulse in SIMION. Figure 33 and Figure 34 show the results obtained from the simulations. The pulse amplitude and width were optimized to reduce the KE of the electrons below 0.2 eV. Once electron KEs were reduced, the trapping efficiency also improved.

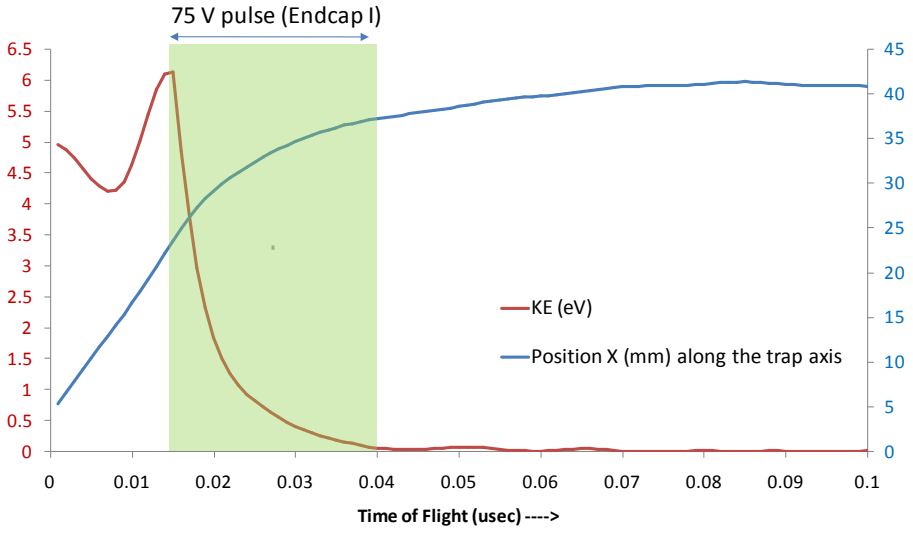


Figure 33: A plot of KE and position of an electron as it enters the trap geometry. Application of a short positive voltage pulse reduces the energy to below 0.2 eV approximately at the center of the trap.

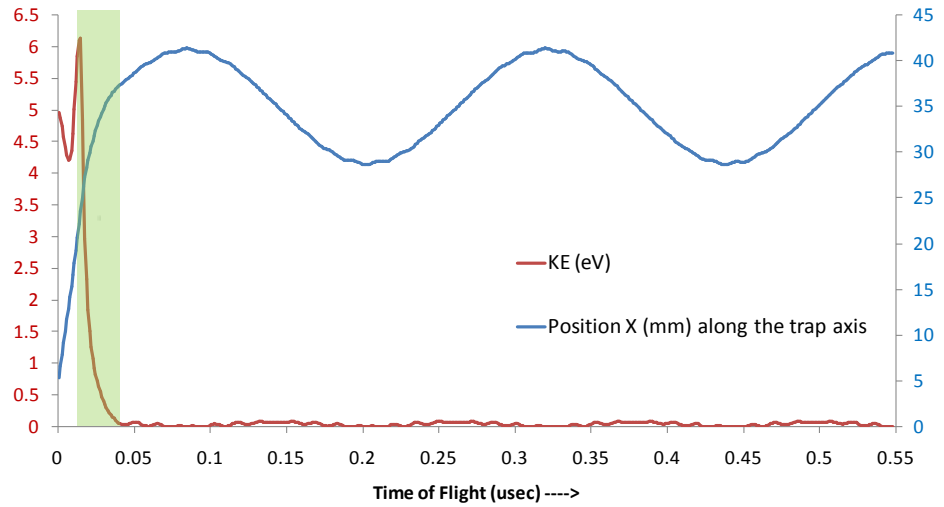


Figure 34: A plot of the KE and position of an electron with respect to time of flight. KE is reduced to below 0.2 eV by a voltage pulse scheme as the electron enters the trap, and the electron maintains low energy thereafter.

Several ranges of electron energies were used to determine the optimum pulse amplitude and width. Table 5 shows examples of pulse widths and amplitudes that successfully slowed electrons using a mesh-type end cap at a distance of 18.5 mm from the trap. Simulations also indicated that more than one combination of pulse amplitude and width could be used for the same energy range. In simulations, electrons in a narrow energy range (±2%) were flown into the trap (in a batch of 50 electrons) and the pulse was applied immediately after they entered the trap. However, in real experiments, the electron source would generate a constant beam of electrons with a range of energies. Thus the timing of the pulse would not be critical, as the center volume of the trap would have a continuous flux of electrons along the entire axis.

Table 5: Examples of pulse parameters (determined in SIMION) used to reduce KE of electrons for a range of electron energies

Electron energy (eV)	Pulse voltage (V)	Pulse width (ns)
0.25	25	7.5
0.5	25	7.5
1.25	25	15
2.5	45	15
5	75	25
10	90	30
15	110	35

As the electron energy was increased beyond 15 eV, it was difficult to slow down electrons within the length of the trapping region without using very short pulses of very high voltage, which becomes challenging experimentally. However, the energy distribution from the microchannel plate (MCP)-generated electrons showed that most of the electrons were in the

range of 1 to 10 eV (see Section 5), and hence this approach could be used to slow down electrons from a MCP with reasonably simple driving electronics.

Simulations showed that cooling was possible using both vertical 3D mesh-type end caps and 2D surface-type end caps. In the case of surface-type end caps, the distance of the pulsed electrode from the trap entrance is much smaller, thus requiring lower voltages (<10 V) to cause the same deceleration of electrons. Both approaches were tested during trap performance evaluation.

4. Fabrication

We adopted a micromachining approach to build the electron trap, which was constructed of two symmetrical parts that we coupled using metal spacers. A Si substrate was used for the supporting structure, and metal layers were patterned using a photolithography technique to obtain the surface electrodes. The length of the metal spacers defined the gap between the surface electrodes on the two Si plates. Figure 35 shows a 3D visualization of the Si chip with the patterned metal electrode layers. Four holes were etched in the Si chip at each corner to allow mounting of the chips with other components in the experimental test setup.

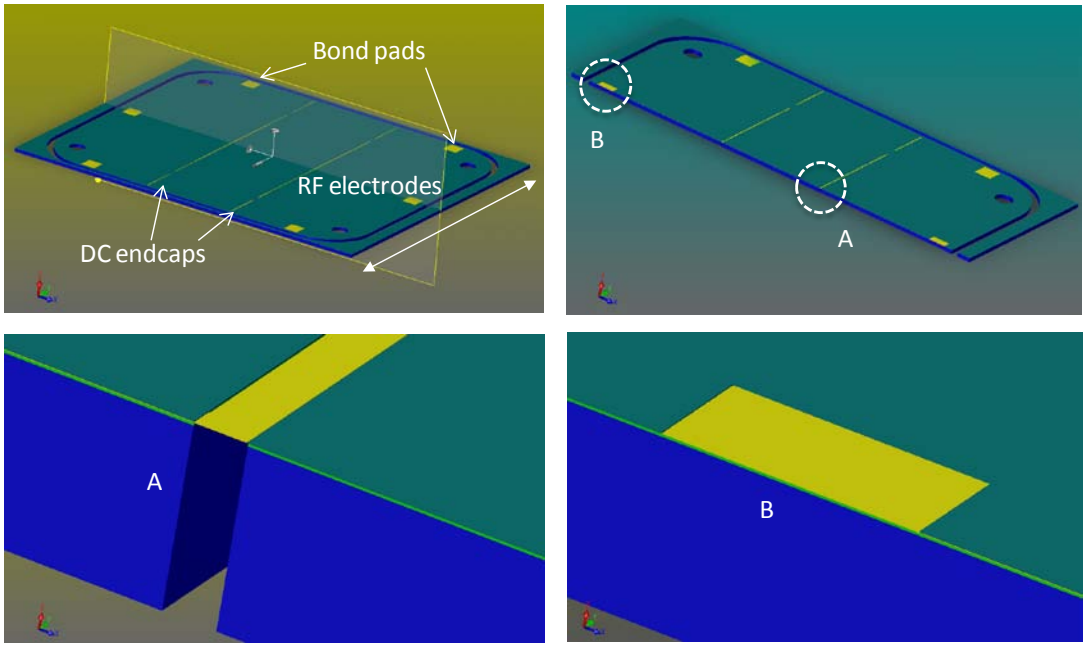


Figure 35: A 3D model of surface electrodes on a Si chip. Four sets of electrodes could be fabricated on one wafer.

For the substrate we used 400-µm-thick N-type (100) 1-10 Ω.cm DSP Si wafers. Since the primary purpose of the Si was to be a supporting substrate for lithography and other MEMS processes, the resistivity and crystallographic orientation were not considered to be critical parameters. Optical mask layouts were designed in Coventor and produced at Photo-sciences, Inc. Figure 36 shows the mask details. The 3-layer mask set was designed for 4-in. Si wafer processing and included two chips each of two different designs: Design I with end-cap electrodes perpendicular to RF electrodes; and Design II with end-cap electrodes aligned with RF electrodes, as depicted in Figure 36.

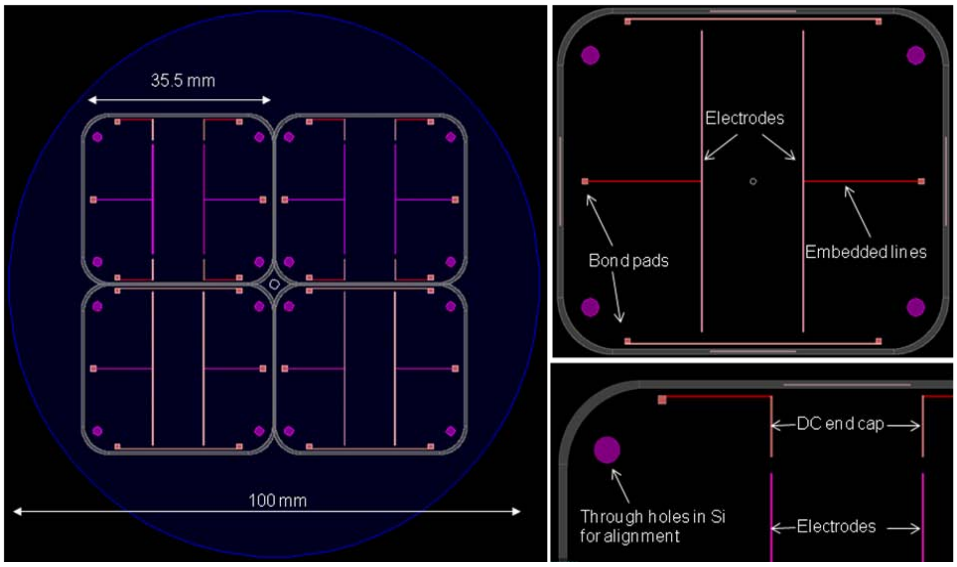


Figure 36: Electron trap mask layout. Left: Overview; Top right: Si chip (Design I); Bottom right: Zoom-in (Design II).

5. Testing

The test setup was constructed to fit in an existing 6x4x3 in^3 aluminum vacuum chamber with a turbomolecular pump and a roughing pump, which were used to obtain a vacuum level of approximately 1e-7 Torr. The vacuum chamber was equipped with four NW16KF electrical feed-throughs, including two high-voltage vacuum feed-throughs and a micro ion gauge to measure low pressures. All the components inside the chamber were installed using eV parts. Figure 37 shows a 3D rendering of the electron trap test setup.

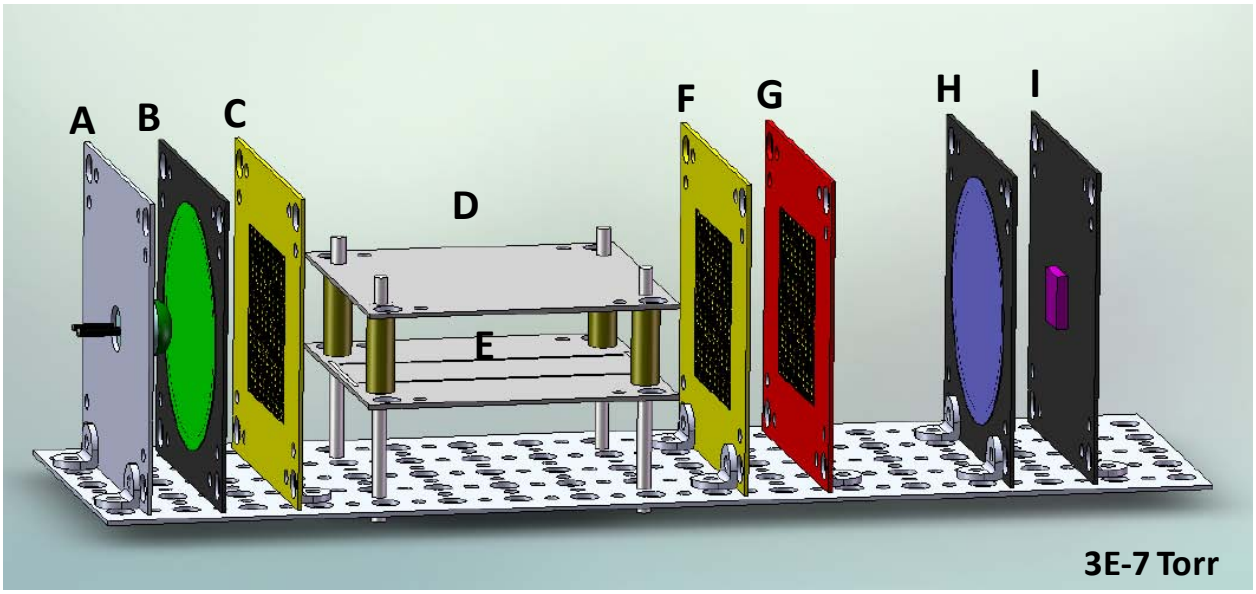


Figure 37: Electron trap test setup showing A) UV LED (255 nm); B) MCP (for electron generation); C) Mesh 1; D) electron trap assembly; E) electron trapping region; F) Mesh 2; G) retardation/acceleration grid; H) phosphor screen; I) silicon photomultiplier (SPM).

A UV light-emitting diode (LED) was used to illuminate a microchannel plate (MCP) to create a pulsed source of electrons, as shown in Figure 37 (A and B). High-transparency nickel meshes (C and F) were installed on both sides of the electron trap assembly (D) to shield the electric field inside the trap (E) from any perturbations from the adjacent high voltage components. An acceleration grid (G) was installed to the right of Mesh 2 to accelerate ejected electrons, if needed. Initially, a high-luminosity phosphor screen was installed to convert electrons ejected from the trap into photons. A high-transparency mesh was installed close to the phosphor screen to accelerate the electrons to energy levels of >500 eV to achieve a reasonable conversion efficiency of electrons to photons on the phosphor screen. A silicon photomultiplier (SPM) was placed on the other side of the phosphor screen for detection of photons generated by the impinging electrons on the phosphor screen. A mu-metal shield was designed and fitted around the electron trap assembly, as shown in Figure 38, to minimize the effect of any stray magnetic and electric fields that might be present in the vacuum housing.

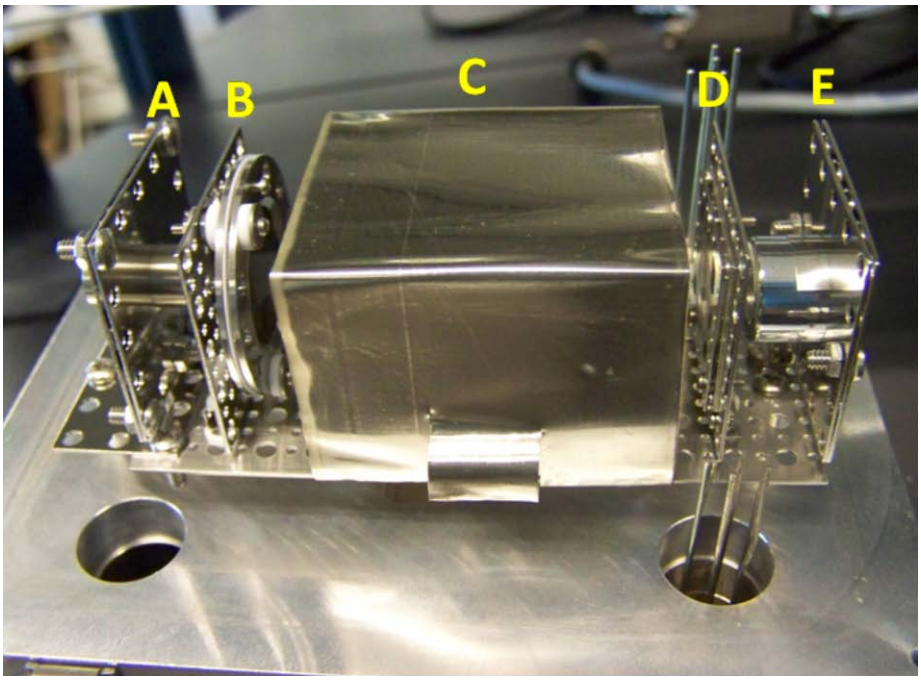


Figure 38: Photograph of the electron trap test setup. A) UV LED source; B) MCP; C) mu-metal shield enclosing the electron trap assembly with a nickel mesh on both sides; D) phosphor screen with nickel mesh on the left; E) tube casing into which the SPM was installed.

After initial tests using the phosphor screen/SPM detection scheme, it was decided that the detection efficiency was insufficient for detection of small numbers of electrons. Consequently, to improve detection sensitivity, the phosphor screen and SPM were replaced with a MCP assembly and anode (H and I in Figure 39, respectively). The electron impact side of the MCP was biased at 100 V, and the backside at 2000 V. The signal from the anode (biased at 100V relative to the backside of the MCP) was amplified using a current amplifier.

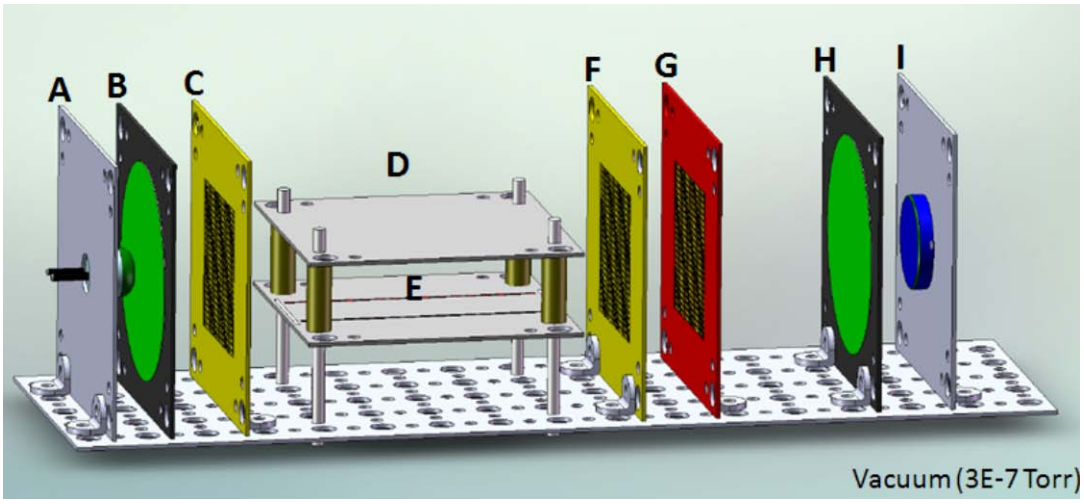


Figure 39: The modified test setup where the phosphor and SPM were replaced by an MCP (H) and an anode plate (I) for electron detection.

After some initial testing that failed to demonstrate trapping of electrons, further advanced simulations indicated that there was a potential penetration into the trapping region from high voltage components. The test setup was thus modified by installing two aluminum (Al) flanges to obtain three separate sections inside the vacuum housing as shown in Figure 40. High-transparency Ni meshes were installed on Al flange machined windows to improve pumping efficiency throughout the chamber, since the turbo pump was installed on one end of the chamber. Components were mounted on the Al flanges and a thicker mesh was installed over the edges of the Al flange for a tight fit against the chamber wall to prevent any small gaps through which the potential might penetrate into the trapping region.

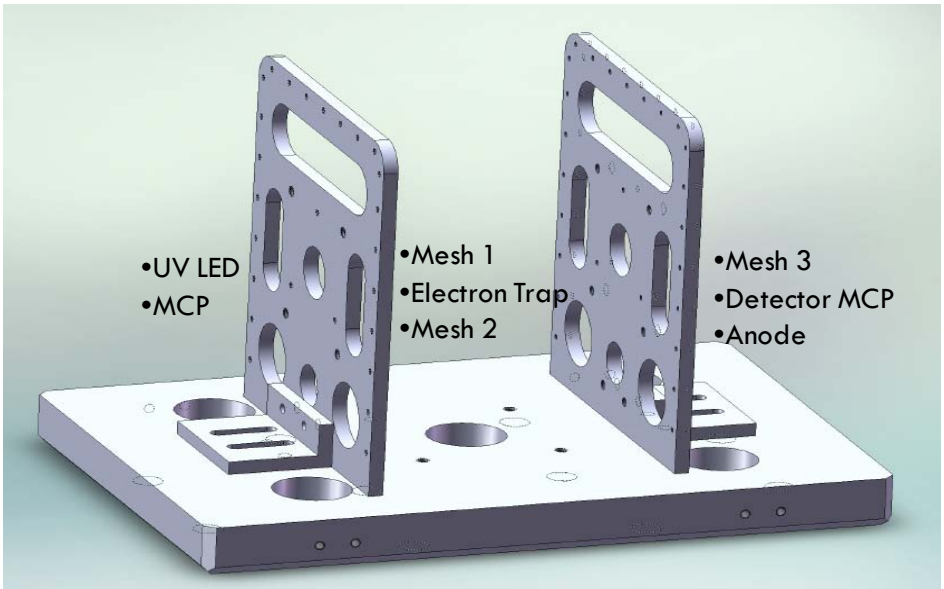


Figure 40: A 3D rendering of the new mounting approach using two Al flanges to reduce the potential penetration into the trapping region from high-voltage components.

Figure 41 and Figure 42 illustrate the arrangement of the electronics used to test the electron trap. To obtain the RF voltages for the trapping electrodes, the signal from a voltage-controlled oscillator was amplified using a class A/AB 8-W broadband power amplifier. To generate a 180° out-of-phase RF signal for the opposite electrodes, the signal from the amplifier was fed into an in-house designed balun circuit. The balun was built by winding a 24-AWG enamel-coated wire to form the primary and secondary winding around an iron powder core. The secondary winding had twice as many turns as the primary and was center-tapped to ground, while the outputs across the two ends of the secondary winding were 180° out of phase.

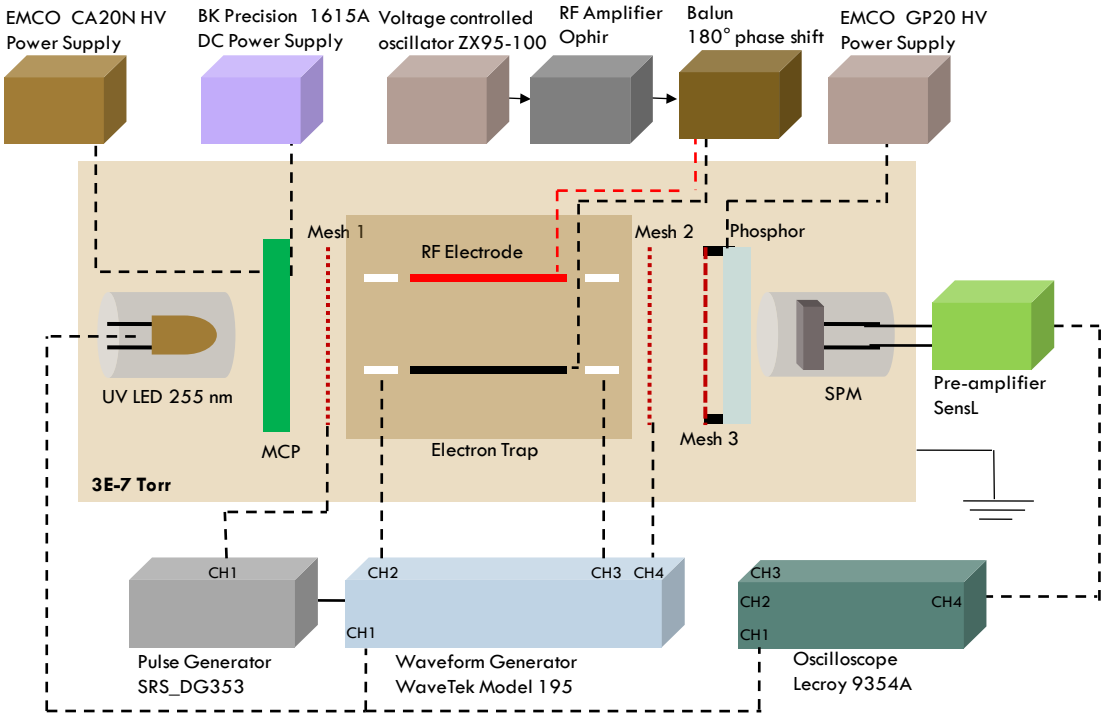


Figure 41: Schematic of electronics used to operate the electron trap test setup

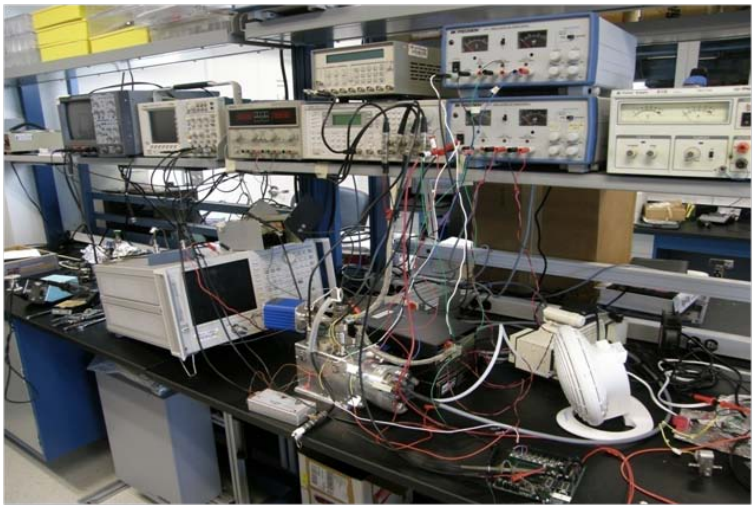


Figure 42: A photograph of the laboratory setup showing the electronic components and the vacuum chamber containing the electron trap setup.

A circuit to generate nanosecond pulses was designed for the pulsed cooling scheme using avalanche transistors 2N2369. The operation of the circuit was based on the fast switching of avalanche transistors. A voltage (V), slightly higher than twice the avalanche voltage of 2N2369, was applied across the three transistors. As soon as a trigger was applied to the base of transistor Q3 to turn it on, it behaved as a short circuit, applying the entire voltage (V) across Q1 and Q2. This led to an avalanche breakdown in Q1 and Q2, thereby resulting in a nanosecond pulse at the output. We changed the width and amplitude of the output pulse by adjusting the values of the resistors and capacitors in the circuit.

6. Results

Simulations

Simulations indicated that electrons can be trapped radially by surface-type electrodes with application of an RF potential. Two different bias configurations were simulated: (1) one in which RF potential was applied to two diagonally opposite electrodes and the other two electrodes were grounded; and (2) instead of grounding the other electrodes, a 180° out-of-phase signal was applied to these electrodes. Simulations indicated that both configurations could be used to trap electrons. Application of a small negative potential on the two surface-type end caps contained the electrons axially. Although both electrode designs (one with end caps aligned with RF electrodes, and the second with end caps perpendicular to RF electrodes) seem to contain electrons inside the trap, the former configuration trapped for a longer time in the simulations. It was also possible to trap electrons in curved geometries, which would be useful for the design of longer traps (e.g., a serpentine or spiral design on a Si wafer) to increase the trapping volume. Electrons could also be trapped in two sections separated by a small gap. The longest trapping time observed was about 159 ms, but it is anticipated that the simulated trapping time could be longer with provision for more accurate simulations.

A pulsed scheme was devised and simulated to cool electron energies to below 0.2 eV. Electrons in a range of electron energies (up to 15 eV) were slowed down by adjustments in the pulse width and amplitude. This method seemed to be very crucial for trapping electrons with high initial energy once they enter the trapping region.

Fabrication

The electron trap fabrication process was optimized over several fabrication and packaging runs. Removal of Si under the area of RF electrodes by means of DRIE resulted in low capacitance (29 pF) but also rendered the Si chip fragile. Mechanical failure modes were observed at multiple steps following the through-wafer etch. The thickness of the Si_3N_4 layer was adjusted to 4 μm to obtain a mechanically rugged membrane that could survive the vibrational and thermal shocks of the mounting and dicing steps. Mounting techniques were improved to ensure strong adhesion to the carrier wafer and easy demounting after the device wafers were diced into individual chips.

A highly resistive semiconducting layer was deposited on top of the SiO_2 layer to ensure that the surface does not charge up due to electrons that may impinge on the surface during trap operation. To achieve this, we conducted a few short-loop experiments to characterize a recipe of atomic layer deposition (ALD) of zinc oxide (ZnO). ALD offers a unique, controlled method of depositing highly uniform thin films at relatively low temperatures on a variety of substrates and surface topography. Figure 43 shows a ZnO film deposited on a SiO_2-coated substrate.

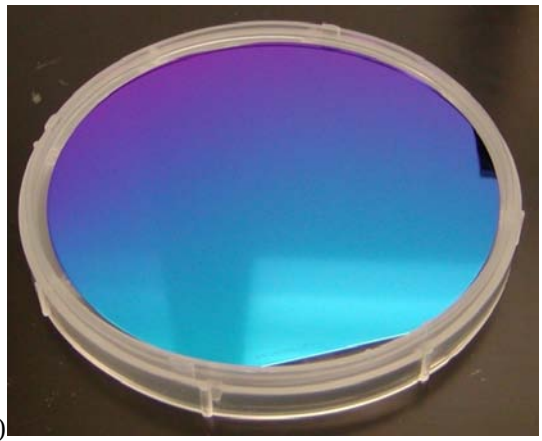
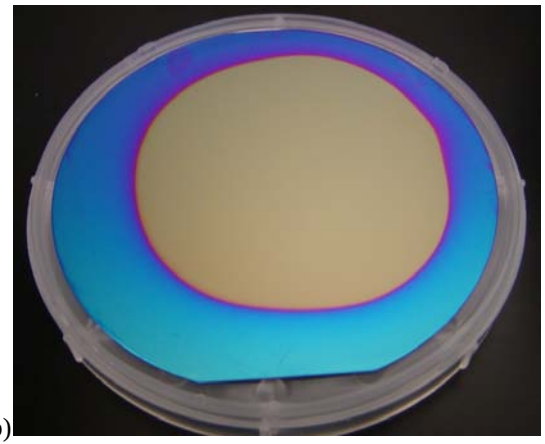
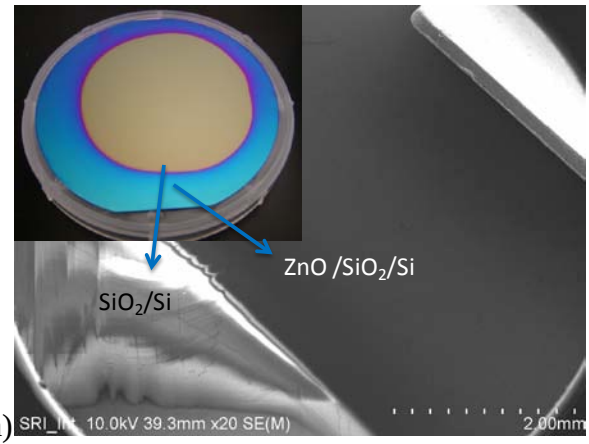
a)  b) 

Figure 43: An image of an oxidized Si wafer after deposition of ZnO using an ALD system at 100°C for 500 cycles of diethyl zinc (DEZ) as the precursor; a) Top side of the wafer; b) Backside of the wafer showing deposited ZnO, demonstrating the highly conformal deposition in the ALD system.

To determine if the ZnO layer dissipated the charge sufficiently, we used a Hitachi (FESEM 4800) SEM to analyze a sample Si wafer that was oxidized before the ZnO deposition. SiO_2 is an insulator and charges up very quickly when exposed to electrons. The backside of the wafer, where ZnO was partly deposited (Figure 43b) was exposed to an electron beam in the SEM. SEM analysis showed that the surface charged up where the ZnO was not deposited, while the surface with ZnO did not charge up, even when the electron energy was increased to 10 keV. Figure 44 shows the SEM images obtained during this experiment.

a) 

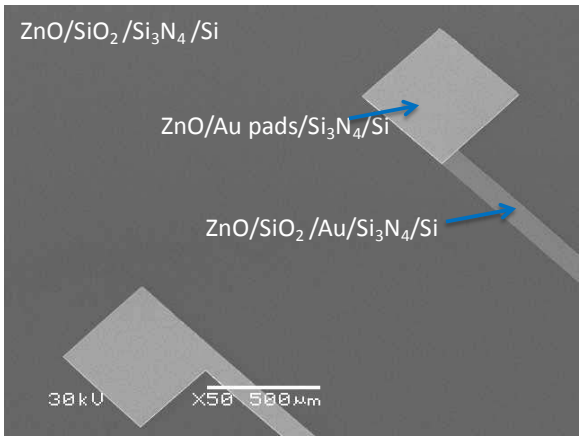
b) 

Figure 44: SEM images of the top surface of the Si wafer; a) A low-magnification SEM of the backside of the wafer showing charge dissipation on the resistive ZnO layer; b) SEM of the ends of the surface electrodes and bond pads of the prototype electron trap.

Electron Source Testing

We conducted experiments to confirm the ability to generate and detect electrons (including short pulses) and characterize the electron energy distribution from the UV LED/MCP source. First, we characterized the MCP-generated electron beam current for a range of potentials applied across the MCP, without switching on the UV LED, by measuring the current on Mesh 1 (Figure 46) with a picoammeter. Some undesirable spontaneous emission occurs inside the MCP

at higher voltages due to self-ionization of gas molecules at regions of high electric field, as represented in Figure 45 (left). Figure 45 (right) shows the measurement of current measured with the UV LED switched on. The blue trace is the actual measurement recorded with the picoammeter, while the red trace is the extrapolated current value based on mesh transparency (80%).

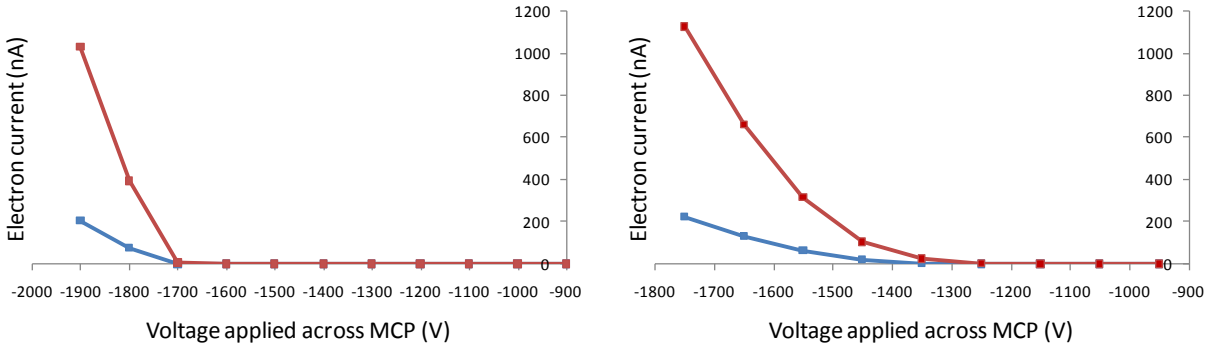


Figure 45: Left: Plot of the electron current vs. potential across the MCP with UV LED turned OFF; Right: Plot of the electron current vs. potential across the MCP with UV LED turned ON

We further characterized the UV LED- and MCP-based electron source using the test setup shown in Figure 46a. To determine the electron energy distribution, the MCP was operated at -1255 V to keep the background current (due to spontaneous emission) at 4 pA or less. The voltage on Mesh 1 was varied to retard the electrons, and the corresponding transmitted electron current on Mesh 2 was recorded using a picoammeter. Figure 46b shows the energy distribution of electrons with the UV LED operated at 99% duty cycle at a pressure of 4.4E-7 Torr inside the vacuum housing. A conclusion from this experiment was that biasing the MCP backside (from which electrons are emitted) at a slightly positive voltage relative to the trapping region will be crucial to keep most of the electrons in the low energy (<10 eV) range for efficient trapping.

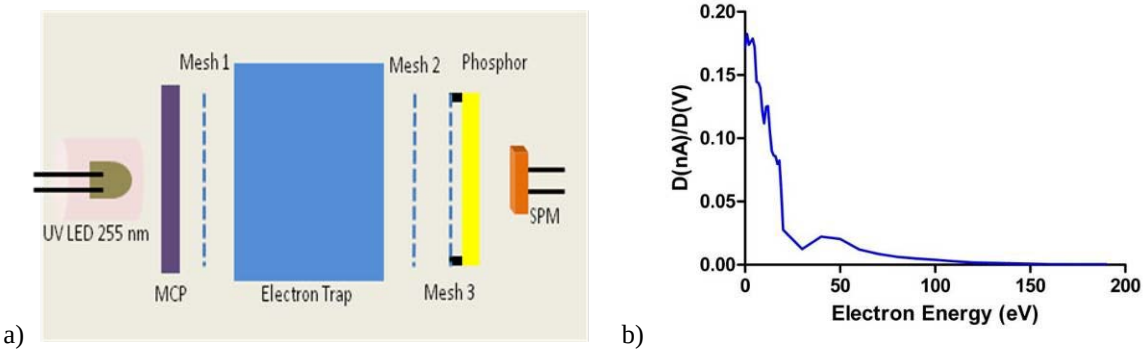
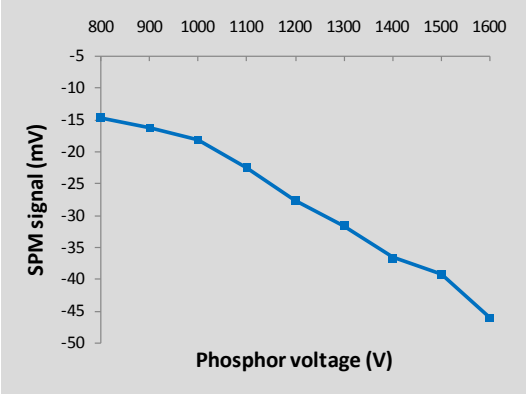


Figure 46: a) Schematic of the test setup; b) Energy distribution of the electrons from the MCP.

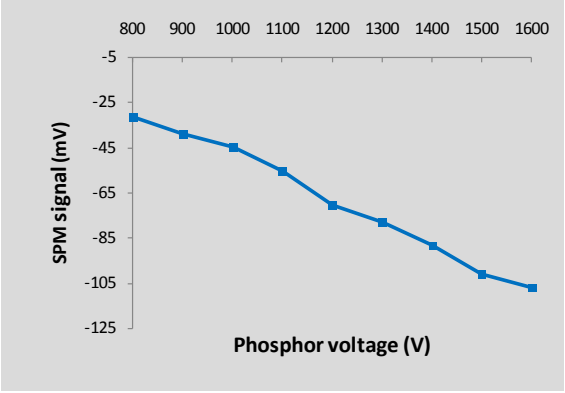
Trapping and Detection

As discussed above, we initially used a combination of phosphor screen and SPM to detect electrons exiting the trap. The phosphor screen was used to convert the impinging electrons into photons, and the photons were detected by the SPM installed behind the phosphor screen, as shown in Figure 46a. Characterization of the detector was performed at two different MCP backside potentials. In Case I (Figure 47 left), the backside of the MCP was grounded and SPM

output signal was measured through an oscilloscope. In Case II (Figure 47 right), the backside of the MCP was kept at -47.9 V and the corresponding SPM output was recorded.



MCP Front: -1450V ; Backside 0 V



MCP Front: -1500 V backside -47.9 V

Figure 47: Left: SPM signal vs. phosphor voltage with the backside of MCP grounded; Right: SPM signal vs. phosphor voltage with the backside of MCP at -47.9 V

As demonstrated by the right plot in Figure 47, biasing the backside of the MCP at slightly negative voltage resulted in higher SPM output signal. Since the potential across the MCP was comparable, the higher SPM output could be attributed to a positive shift in energy of electrons by 47.9 eV, which resulted in improved transmission to the phosphor screen and better conversion to photons on the screen.

To evaluate the ability to detect short pulses of electrons using this detection scheme, the UV LED was operated in a 10-ms pulse-mode to generate photoelectrons. A potential of -1550 V was applied across the MCP to generate secondary electrons, which were accelerated to the phosphor screen by biasing Mesh 3 (directly in front of the phosphor) at 1200 V to create photons. This photon signal was detected by the SPM, which was operated in the avalanche mode, and the signal was recorded on the oscilloscope as represented in Figure 48.

Experiments were performed to investigate the trapping behavior of the electron trap using the phosphor-SPM-based detector. Different DC endplate voltages were used in attempts to confine electrons of varying energy in the trap (1 to 10 eV). No signal was observed when the DC end cap II was lowered to eject any electrons that might have been trapped. To enhance the detection sensitivity of the setup, the

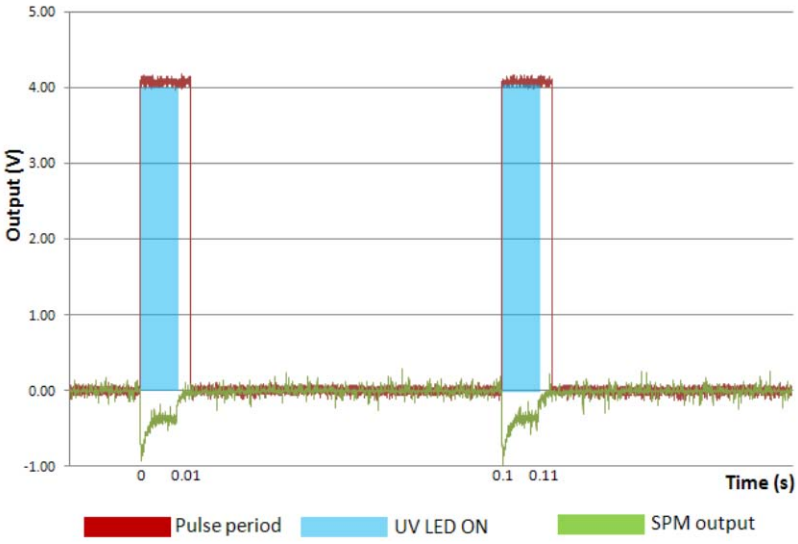


Figure 48: A plot of the SPM signal which confirms the generation and detection of electrons in a short-pulse mode.

phosphor-SPM-based detector was replaced with a MCP-based detector. The appropriately biased MCP amplifies the electron signal and produces a signal that can be detected through a current amplifier fed through a small “pickup” capacitor. The sensitivity obtained using the MCP-based detector was found to be over 2500 times higher than that obtained using phosphor and SPM detectors. The MCP-based detector also improved the response time, as it was determined that the phosphor had an inherent time delay, due to the time required for the electron charge to dissipate. Connections in the test setup were re-routed to reduce the pickup on the anode detector from other timing pulse signals. A -1500 V bias was applied at the MCP (electron source) while a +1000 V bias was applied at the MCP (detector). Meshes 2 and 3 were grounded and Mesh 1 was connected to a picoammeter to record the electron current.

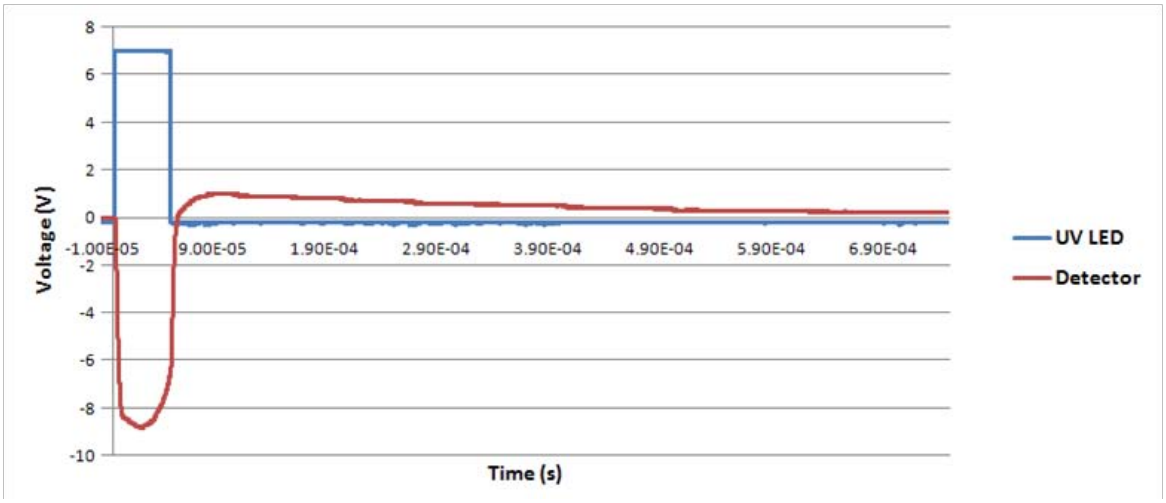


Figure 49: A plot of the MCP-based detector response for an electron current of 3.8 nA.

Many variables were adjusted to attempt to trap, eject, and detect electrons; however, none of these experiments were successful. Section 7 outlines what we consider to be the outstanding issues and possible solutions for obtaining an ultimately successful demonstration of electron trapping using a planar LIT.

7. Critical Issues and Solution Paths

1. Electrons are very light and easily influenced by stray electric and magnetic fields. The magnetic field being generated by the turbo pump could also be an issue to resolve. Proper magnetic shielding will be required to ensure minimum magnetic interference.
2. The detector loses sensitivity immediately (50-100 μs) after it recovers from the intense electron beam signal during the “fill” cycle for the trap. This recovery time overlaps the time during which electrons are expected to be ejected from the trap. The main electron beam signal during operation of the UV LED will need to be blocked by application of negative potential on Mesh 3 to avoid saturation of detector (electronics need to be purchased or developed for this).
3. Verification and evaluation of the trapping potential generated by the planar LIT by generating and trapping ions instead of electrons (which are much heavier and require a lower frequency trapping RF voltage) would be useful to determine whether the trap is functioning according to simulations.

8. Future Directions

Once electron trapping is experimentally verified using the existing planar LIT, more sophisticated trap configurations should be investigated. We demonstrated through simulations that a pulsed scheme could be used to fill small trap sections of a much longer electron trap sequentially by using small end-cap voltages. A conceptual design is illustrated in Figure 50, where a long trapping region is defined by photolithographically patterned high-precision metal surface electrodes on Si wafer. MEMS technology can be used for both fabrication and assembly to build such a structure with high alignment accuracy. A high-volume charged-particle storage approach could be developed by using a stack of multiple Si wafers with trapping regions designed between each wafer, with transfer of electrons between wafers made possible through pulse scheme manipulation. Limitations due to space-charge effects can be reduced by designing tracks of electron traps laterally separated from each other by some gap, as shown in Figure 50. Such a design could be used to attain high storage capacities that have not been possible before now, and could be applied to develop a portable positron source.

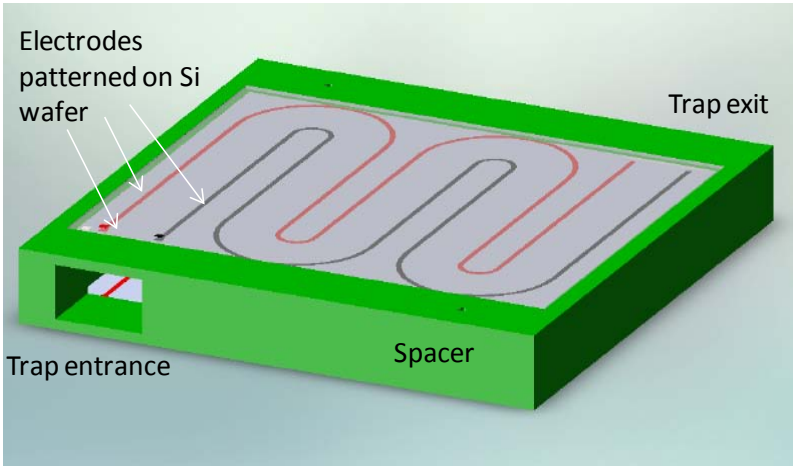


Figure 50: Illustration of an advanced conceptual trap design to increase the trapping volume by increasing the length of the trap.

9. References

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DESCRIPTION OF CONTRACT DELIVERABLES

Task	Quantity	Description
1.1	10	Prototype MEMS-based circuit breaker, 44-pin package
1.2	1	Prototype MEMS-based voltage converter, 44-pin package
1.3	1	Nanocrystalline diamond thin film, 1.72 μm thick, deposited on Si(100) substrate
	1	Microcrystalline diamond substrate, freestanding, ~350 μm thick, double-side mechanical polish
2	4	MEMS electron trap structures fabricated on Si wafers